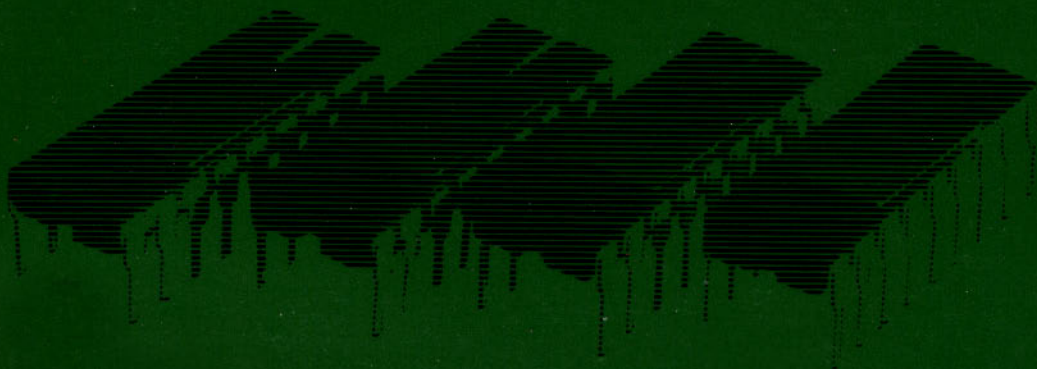


HIGH SPEED DATA PROCESSING INTEGRATED CIRCUIT HANDBOOK

# HIGH SPEED DATA PROCESSING INTEGRATED CIRCUIT HANDBOOK



**PLESSEY**  
Semiconductors



 PLESSEY

**HIGH SPEED  
DATA PROCESSING  
INTEGRATED  
CIRCUIT  
HANDBOOK**



Designed and produced by Peter Wigen Consultants  
© The Plessey Company plc  
December 1983  
Publication No. P.S. 1989

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\* The SP16F60, SP16F70, SP9131, SP9685 and SP9687 are pin-compatible higher performance versions of the equivalents shown.

# Quality data

Plessey Semiconductors has Factory Approval to:-

**BS9300** for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)

**BS9400** for integrated circuits of Assessed Quality (BSI Certificate 1053/M)

**CECC 50000** Inspection Organisation to document level 1 (BS9300) M0020/CECC refers

**DEF STAN 05 — 21 QC** System requirements for Industry (Equivalent to AQAP — 1) Certificate 65752/1/01 refers

Devices are also manufactured and tested in accordance with the methods of **MIL-STD-833**, the US Military Standard; Test Methods and Procedures for Microcircuits, and **MIL-M-38510**, US Military Specification, Micro-electronics; General Specifications for.

# Ordering information

All Plessey Semiconductors integrated circuits are allocated type numbers which must be quoted when ordering. This number may or may not have a suffix (A, B, C, etc.) which denotes the precise electrical specification or temperature grade. When there is a choice of packages the two-digit Pro-Electron code is used to identify the style required, according to the following table:

- CM** - Multilead TO-5
- DC** - Ceramic Dual-in-Line (metal lid)
- DG** - Ceramic Dual-in-Line

Within the UK, orders for quantities up to 99 will be referred to your local Distributor. Quantities of 1000 and over must be ordered from:

**Plessey Semiconductors Limited**  
**Cheney Manor**  
**Swindon, Wiltshire SN2 2QW**  
**United Kingdom**  
**Telephone: Swindon (0793) 36251**  
**Telex: 449637**

A reciprocal arrangement exists with all Distributors, but it will expedite delivery of order if buyers can direct orders as indicated above. Outside the UK, irrespective of quantity, you are invited to contact your nearest Plessey Semiconductors Sales Outlet (see pp. 109-111).



### **DELIVERED PRODUCT QUALITY**

It is our policy to deliver a reliable quality product and to achieve this end all devices undergo 100% electrical testing of every relevant AC and DC parameter prior to shipment. The devices are tested under conditions of level and frequency closely simulating those of the typical application. Fully automatic Teradyne integrated circuit test machines, acknowledged to be among the best computer controlled test machines available, are employed.

Each and every stage of processing, assembly and testing is carefully audited by Plessey Semiconductors' independent Quality Assurance department.

Therefore we are able to guarantee the following Acceptable Quality Level (A.Q.L.) on all deliveries.

### **MECHANICAL**

Defects of a mechanical nature including coding not being legible, deformed leads, dimensional tolerances being exceeded, wrong identification of pin 1 and pins not being solderable.

0.65 %AQL, I.L.II

### **ELECTRICAL**

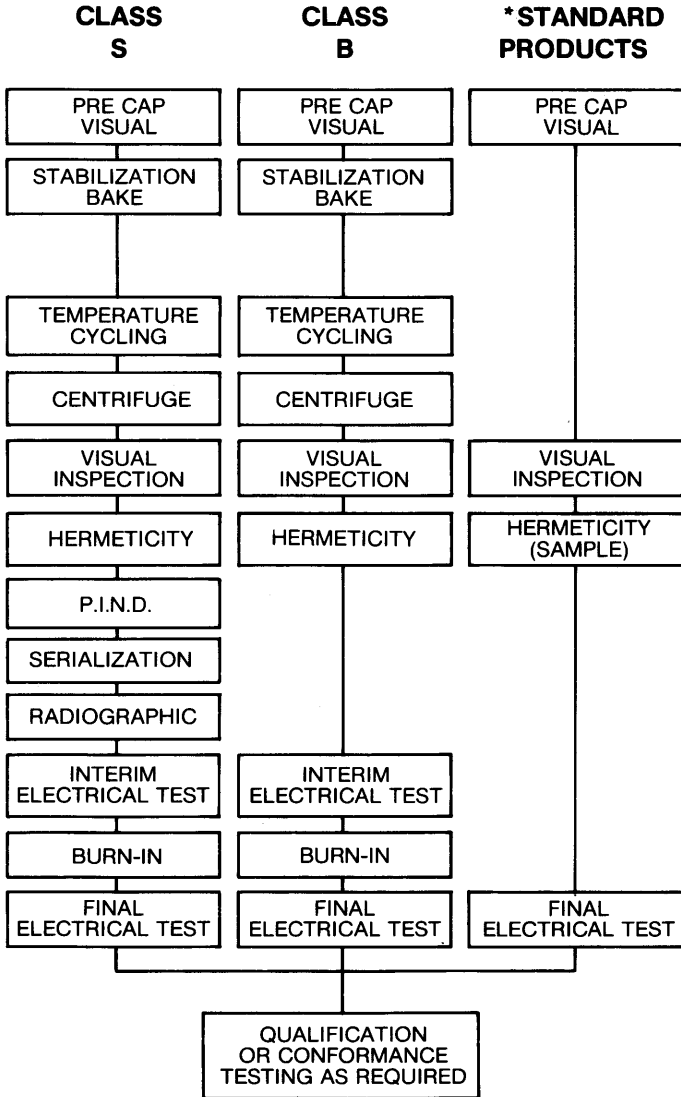
Defects of an electrical nature including device parameters being outside the acceptance specification limits, or those only stated as typical being grossly in error.

0.4 %AQL, I.L.II

The average delivered product quality is considerably better than this, the population of imperfect devices being much smaller than that indicated by the AQL values.

# Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



\*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.







# **Technical Data**

## **NOTE**

**ECL power supplies are nominally +5V, -5.2V unless stated otherwise. Supply tolerance of  $\pm 0.25\text{V}$  will give correct functional operation. Electrical characteristics are measured at nominal supplies.**

# SP705B

## CRYSTAL CONTROLLED INTEGRATED CIRCUIT OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency  $f$  as follows:  $f/2$ ,  $f/4$ ,  $f/2$  and  $f/4$ . The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications.

### FEATURES

- Operating Frequency up to 10MHz
- $f/2$  and  $f/4$  Outputs
- 4 TTL Level Outputs
- Operates from +5V TTL Supply

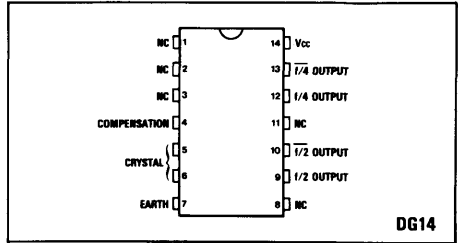


Fig.1 Pin connections

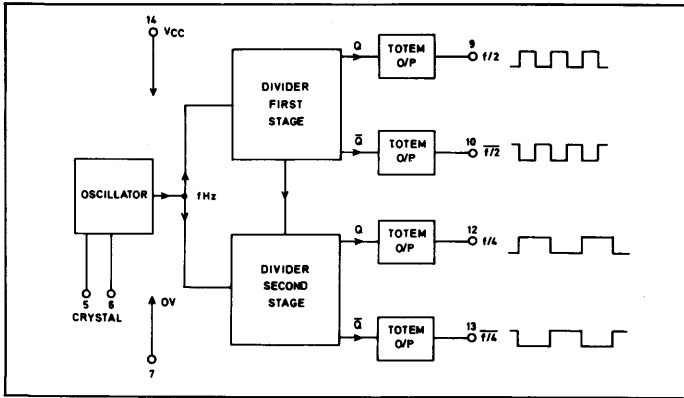


Fig.2 SP705B block diagram

### ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):  
 $V_{CC} = +5V$

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
High state output voltage	$V_{OH}$	2.6		V	$V_{CC} = 4.75V$ $I_{OH} = 0.2mA$
Low state output voltage	$V_{OL}$		0.4	V	$V_{CC} = 5.25V$ $I_{OL} = 8mA$
Supply current	$I_{CC}$		35	mA	$V_{CC} = 5V$
Output rise time (10 % to 90 %)	$t_R$		20	ns	$V_{CC} = 5V$
Output fall time (90 % to 10 %)	$t_F$		20	ns	$V_{CC} = 5V$
Operating frequency (f)			10	MHz	
Operating temperature range		0	70	°C	



# SP705

## CIRCUIT DESCRIPTION

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with a 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig.3.

The circuit is designed to provide low crystal drive levels - typically, less than 0.15mW at 5MHz. This is well within crystal manufacturers' limit of 0.5mW.

The compensation point, pin 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

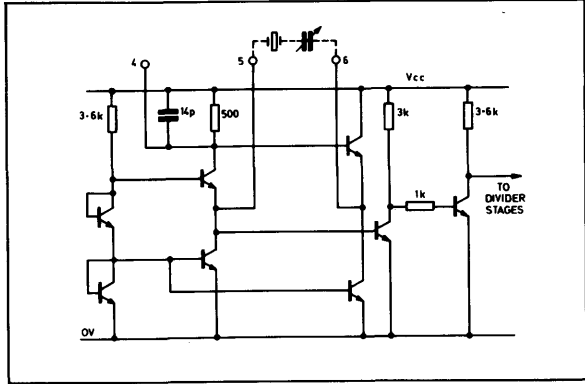


Fig.3 Circuit diagram of SP705B oscillator

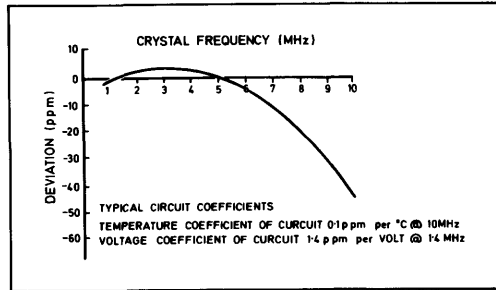


Fig.4 Deviation from nominal crystal frequency

# SP1648

## VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

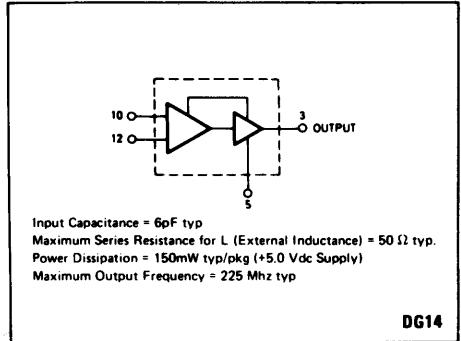


Fig. 1 Block diagram of SP1648

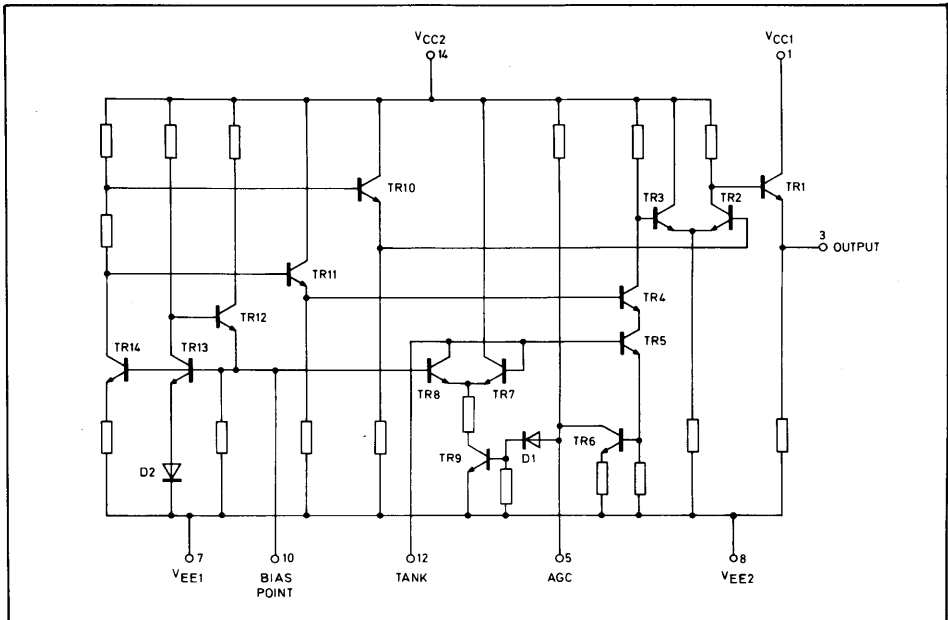


Fig. 2 Circuit diagram of SP1648

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply Voltage = +5.0 volts

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits						TEST VOLTAGE/CURRENT VALUES		V <sub>I</sub> (Gnd)			
			-30°C		+25°C		+85°C		I (mA)					
			Min	Max	Min	Max	Min	Max	V <sub>IH</sub> max	V <sub>IH</sub> min		V <sub>CC</sub>	I <sub>L</sub>	
Power Supply Drain Current	I <sub>CC</sub>	8	3.84	4.18	4.04	4.25	4.11	4.36	—	12	1.14	3	7.8	
Logic "1" Output Voltage	V <sub>OH</sub>	3	3.16	3.40	3.20	3.43	3.23	3.46	V <sub>CC</sub>	—	1.14	3	7.8	
Logic "0" Output Voltage	V <sub>OL</sub>	3	1.51	1.86	1.40	1.70	1.28	1.58	V <sub>CC</sub>	—	1.14	—	7.8	
Peak-to-Peak Tank Voltage	V <sub>pp</sub>	12	—	—	—	—	—	—	—	—	—	1.14	3	7.8
Dutty Duty Cycle	V <sub>DC</sub>	3	—	—	—	—	—	—	—	—	—	1.14	3	7.8
Distortion Frequency	F <sub>max</sub>	—	—	—	200	225	—	—	—	—	—	1.14	3	7.8

① Test Temperature  
-30°C  
+25°C  
+85°C

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	1.14	—
—	12	1.14	3
12	—	1.14	3
—	—	1.14	—

② Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	1.14	—
—	12	7.8	—
12	—	7.8	3
—	—	7.8	—

③ Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

④ Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

⑤ Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

⑥ Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

\*This measurement guarantees the dc potential at the test point for purposes of incorporating a vector turning diode at this point.

Supply Voltage = -5.2 volts

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits						TEST VOLTAGE/CURRENT VALUES		V <sub>CC</sub> (Gnd)			
			-30°C		+25°C		+85°C		I (mA)					
			Min	Max	Min	Max	Min	Max	V <sub>IH</sub> max	V <sub>IH</sub> min		V <sub>CC</sub>	I <sub>L</sub>	
Power Supply Drain Current	I <sub>CC</sub>	8	1.045	-0.815	-0.960	-0.750	-0.890	-0.650	V <sub>CC</sub>	—	7.8	3	1.14	
Logic "1" Output Voltage	V <sub>OH</sub>	3	1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V <sub>CC</sub>	—	7.8	3	1.14	
Logic "0" Output Voltage	V <sub>OL</sub>	3	-3.090	-3.340	-3.800	-3.500	-3.920	-3.620	V <sub>CC</sub>	—	7.8	—	1.14	
Peak-to-Peak Tank Voltage	V <sub>pp</sub>	12	—	—	—	—	—	—	—	—	—	7.8	3	1.14
Dutty Duty Cycle	V <sub>DC</sub>	3	—	—	—	—	—	—	—	—	—	7.8	3	1.14
Distortion Frequency	F <sub>max</sub>	—	—	—	200	225	—	—	—	—	—	7.8	3	1.14

① Test Temperature  
-30°C  
+25°C  
+85°C

TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

② Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

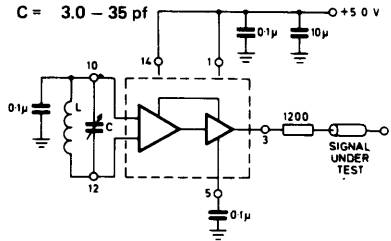
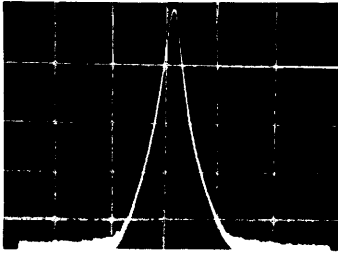
③ Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

④ Test Temperature  
-30°C  
+25°C  
+85°C

V <sub>IH</sub> max	V <sub>IH</sub> min	V <sub>CC</sub>	I <sub>L</sub>
—	—	7.8	—
—	12	7.8	3
12	—	7.8	3
—	—	7.8	—

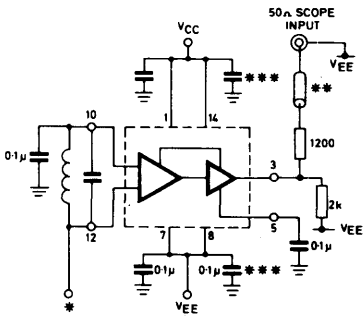
\*This measurement guarantees the dc potential at the test point for purposes of incorporating a vector turning diode at this point.



\* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

B.W. = 10kHz  
Center Frequency = 100MHz  
Scan Width = 50kHz/div  
Vertical Scale = 10db/div

Fig. 3 Spectral purity of signal at output



- \* Use high impedance probe (>1.0 Megohm must be used).
- \*\* The 1200 -ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.
- \*\*\* Bypass only that supply opposite ground.

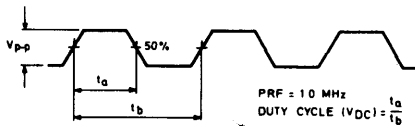


Fig. 4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 thru TR14 provide this bias drive for the oscillator and output buffer. Figure 3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 5), it should be noted that the cathode of the varactor diode (D) should be biased at least  $2 V_{BE}$  above  $V_{EE}$  ( $\approx 1.4$  V for positive supply operation).

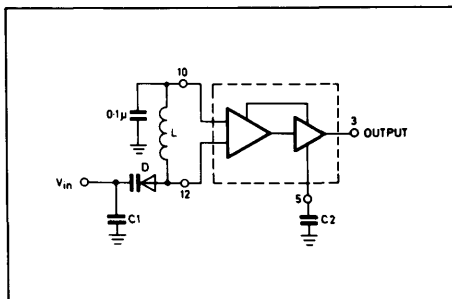


Fig. 5 The SP1648 operating in the voltage-controlled mode

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 6.

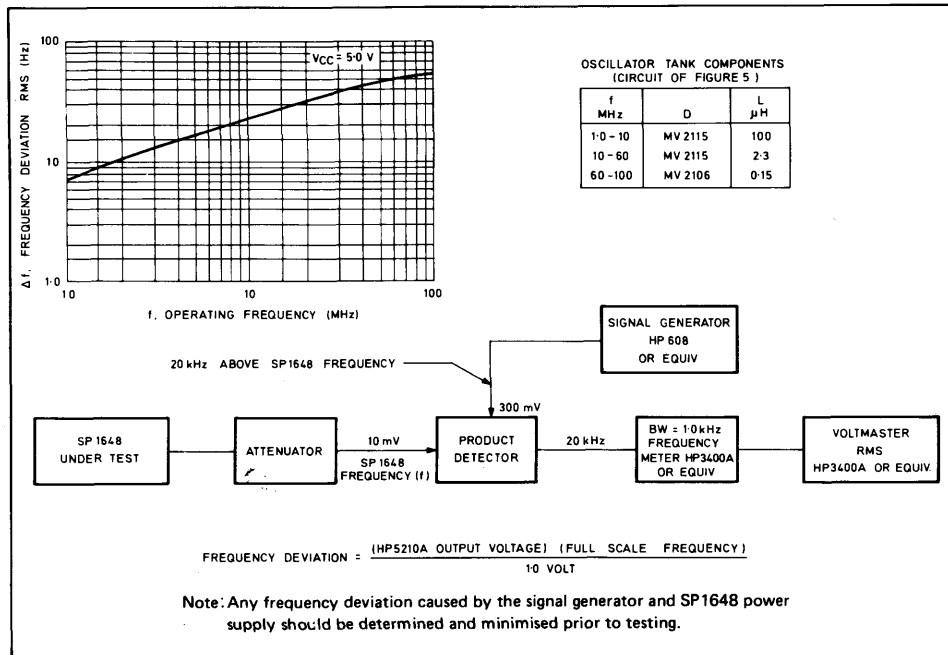


Fig. 6 Frequency deviation test circuit

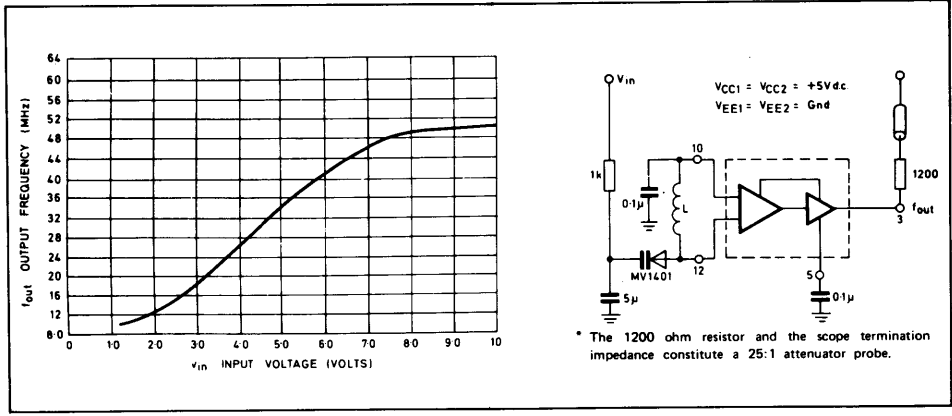


Fig. 7

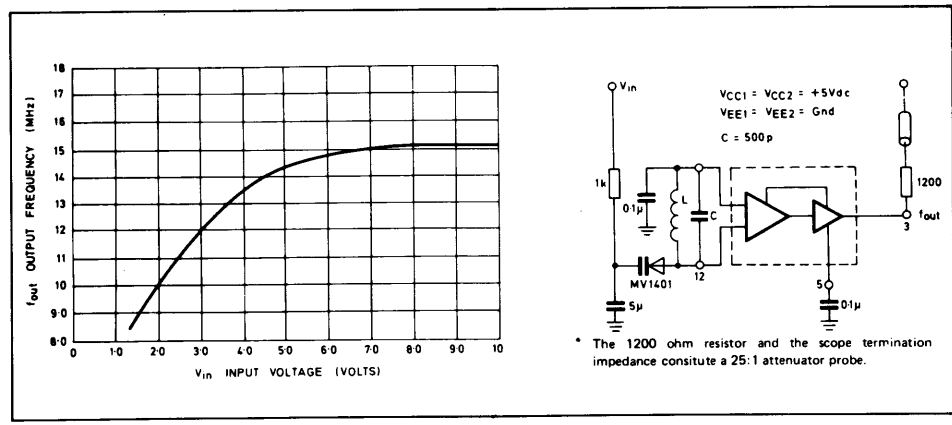


Fig. 8

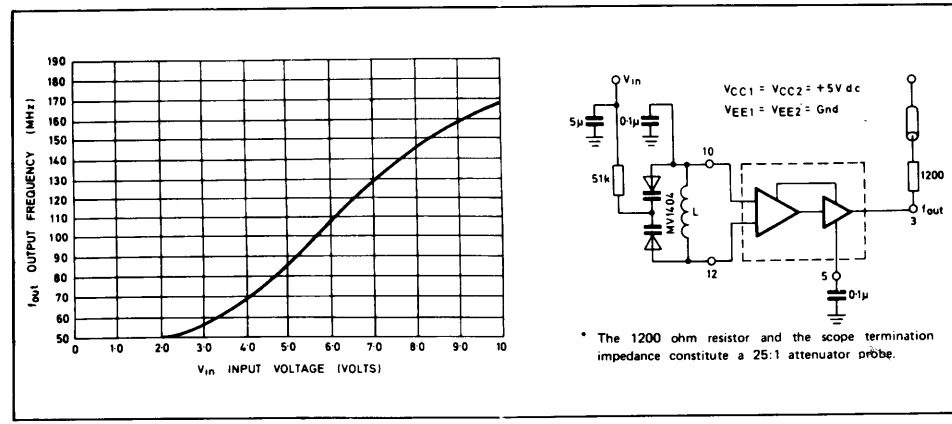


Fig. 9

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 7, 8, and 9. Figures 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6pF typical). Figure 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 k $\Omega$  resistor in Figures 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 k $\Omega$ ) in Figure 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{\max}}{f_{\min}} = \frac{\sqrt{C_D(\max) + C_S}}{\sqrt{C_D(\min) + C_S}}$$

$$\text{where } f_{\min} = \frac{1}{2\pi \sqrt{L(C_D(\max) + C_S)}}$$

$C_S$  = shunt capacitance (input plus external capacitance).

$C_D$  = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Figure 3).

Capacitors (C1 and C2 of Figure 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 $\mu$ F capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used).

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 k $\Omega$  minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used).

# SP1650

## DUAL A/D COMPARATOR

The SP1650 is a very high speed comparator utilising differential amplifier inputs to sense analogue signals above or below a reference level. An output latch provides a unique sample-hold feature.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ( $\overline{C}_a$  and  $\overline{C}_b$ ) operate from ECL III or ECL 10,000 digital levels. When  $\overline{C}_a$  is at a logic high level,  $Q_a$  will be at a logic high level provided that  $V_1 > V_2$  ( $V_1$  is more positive than  $V_2$ ).  $\overline{Q}_a$  is the logic complement of  $Q_a$ . When the clock in to a low logic level, the outputs are latched in their present state.

### FEATURES

- $P_D = 330\text{mW typ/pkg}$  (No Load)
- $t_{pd} = 3.5\text{ns typ.}$
- Input Slew Rate =  $350\text{V}/\mu\text{s}$
- Differential Input Voltage:  $-5.0\text{V to } +5.0\text{V}$  ( $-30^\circ\text{C to } +85^\circ\text{C}$ )
- common Mode Range:  $-3.0\text{V to } +2.5\text{V}$  ( $-30^\circ\text{C to } +85^\circ\text{C}$ )
- Resolution:  $\leq 20\text{mV}$  ( $-30^\circ\text{C to } +85^\circ\text{C}$ )
- Drives  $50\Omega$  lines

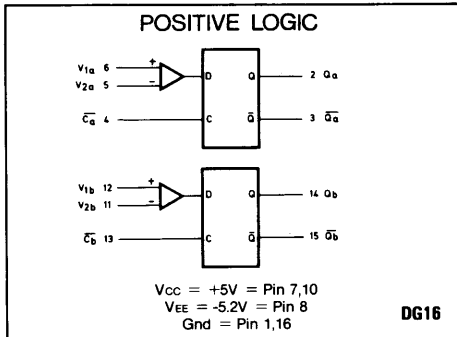


Fig.1 Logic diagram

### TRUTH TABLE

$\overline{C}$	$V_1$ $V_2$	$Q_n + 1$	$\overline{Q}_n + 1$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	$\phi$ $\phi$	$Q_n$	$\overline{Q}_n$

$\phi$  = Don't Care

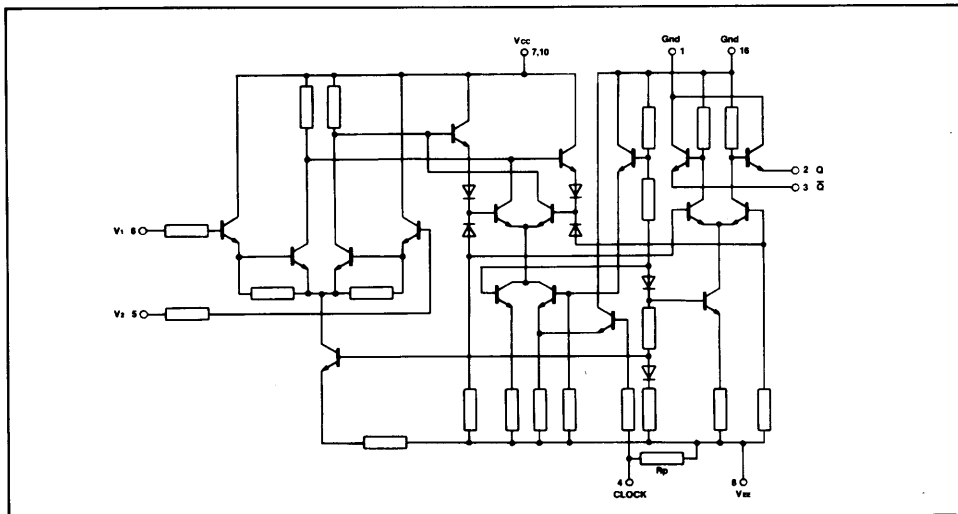


Fig.2 Circuit diagram



**ELECTRICAL CHARACTERISTICS**

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc.

Characteristic	Symbol	Pin Under Test	SP1650 Test Limits (1)						TEST VOLTAGE VALUES (Vohs)										Gnd										
			-30°C		+25°C		+85°C		V <sub>IHmax</sub>		V <sub>IHmin</sub>		V <sub>IHAmx</sub>		V <sub>IHAmn</sub>		V <sub>I1</sub>			V <sub>I2</sub>		V <sub>I3</sub>		V <sub>I4</sub>		V <sub>I5</sub>		V <sub>I6</sub>	
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Min	Max	Min		Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
Power Supply Drain Current	I <sub>CC</sub>	7, 10	-	-	-	-	25*	mAdc	4, 13	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	I <sub>CE</sub>	8	-	-	-	55*	mAdc	4, 13	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
Input Current	I <sub>in</sub>	6	-	-	-	10	μAdc	4	13	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	
	I <sub>r</sub>	6	-	-	-	7	μAdc	4	13	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	
Input Clot Current	I <sub>inH</sub>	4	-	-	-	350	μAdc	4	13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	I <sub>inL</sub>	4	-	-	-	0.5	μAdc	4	13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
Logic '1' Output Voltage	V <sub>OH</sub>	2	-1.045	-0.875	-0.860	-0.810	-0.890	-0.700	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OH1</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OH2</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OH3</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OH4</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OH5</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12
Logic '0' Output Voltage	V <sub>OL</sub>	2	-1.890	-1.650	-1.650	-1.620	-1.830	1.575	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OL1</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OL2</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
	V <sub>OL3</sub>	2	-	-	-	-	-	-	Vdc	4, 13	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	6, 12	
Logic '1' Threshold Voltage	V <sub>OH4</sub>	2	-1.065	-0.980	-	-	-0.910	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
	V <sub>OH3</sub>	3	-	-	-	-	-	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4		
	V <sub>OH2</sub>	3	-	-	-	-	-	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
	V <sub>OH1</sub>	3	-	-	-	-	-	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
Logic '0' Threshold Voltage	V <sub>OL4</sub>	3	-	-1.630	-	-	-1.600	1.555	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
	V <sub>OL3</sub>	3	-	-	-	-	-	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
	V <sub>OL2</sub>	3	-	-	-	-	-	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
	V <sub>OL1</sub>	3	-	-	-	-	-	-	Vdc	13	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4

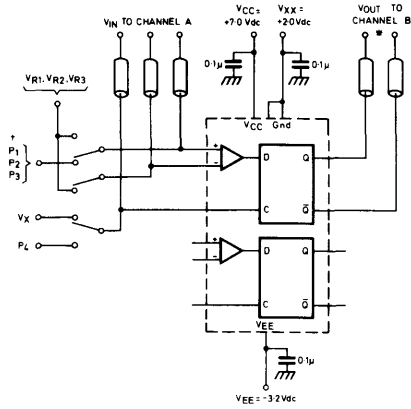
**NOTES**

- All data is for 1/8 SP1650 except data marked (\*), which refers to the entire package.
- These tests done in order indicated. See Figure 6.
- Maximum Power Supply Voltages (beyond which device life may be impaired):  
|V<sub>EE</sub>| + |V<sub>CC</sub>| < 12V dc.
- At all temperatures, V<sub>AS</sub> = +3.000V, V<sub>A4</sub> = +2.980V, V<sub>A5</sub> = -2.500V and V<sub>A6</sub> = -2.480V.

Characteristic	Pin Under Test	TEST VOLTAGE VALUES (Volts)												See Figure 4										
		-30°C						+25°C							+85°C									
		Min		Max		Unit		Min		Max		Unit			Min		Max		Unit					
		VR1	VR2	VR3	VX	VXX	VCC	VEE	P1	P2	P3	P4	VR1		VR2	VR3	VX	VXX	VCC	VEE	P1	P2	P3	P4
Characteristic Switching Times Propagation Delay (50% to 50%) V-Input to Output	16+2+	2	2.0	5.0	2.0	5.7	ns	5	5	-	4	1,11,16	7,10	8	6	-	-	-	6	-	-	-	-	
	16+2+	2	-	-	-	-	-	-	5	5	-	-	-	-	-	-	-	-	-	6	6	-	-	
	16+3-	3	-	-	-	-	-	-	5	5	-	-	-	-	-	-	-	-	-	6	6	-	-	
	16+3-	3	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
	16-2-	2	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
	16-3+	3	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
	16-3+	3	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
	16-3+	3	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
	16-3+	3	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
	16-3+	3	-	-	-	-	-	-	5	5	-	5	-	-	-	-	-	-	-	-	6	6	-	-
14+2-	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	-	-	-	-	-	-	-	-	-	-	6	-	-	4	
14+2-	2	-	-	-	-	-	-	-	6	-	-	-	-	-	-	-	-	-	-	5	-	-	-	
14+3+	3	-	-	-	-	-	-	-	6	-	-	-	-	-	-	-	-	-	-	5	-	-	-	
14+3+	3	-	-	-	-	-	-	-	5	-	-	-	-	-	-	-	-	-	-	6	-	-	-	
testup	6	-	-	-	-	-	-	ns	5	-	-	2.5	-	-	-	-	-	-	-	6	-	-	-	
testup	6	-	-	-	-	-	-	ns	5	-	-	1.5	-	-	-	-	-	-	-	6	-	-	-	
testup	6	-	-	-	-	-	-	ns	5	-	-	1.5	-	-	-	-	-	-	-	6	-	-	-	
Rise Time	12+	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	-	-	-	-	-	-	-	-	-	6	-	-	-	
Fall Time	13+	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	-	-	-	-	-	-	-	-	-	6	-	-	-	
Fall Time	12-	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	-	-	-	-	-	-	-	-	-	6	-	-	-	
Fall Time	13-	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	-	-	-	-	-	-	-	-	-	6	-	-	-	

## NOTES

- Maximum Power Supply Voltages (beyond which device life may be impaired):  
 $|V_{CC}| + |V_{EE}| = 12V$  dc.
- Unused clock inputs may be tied to ground.
- See Figure 10.
- At all temperatures,  $V_{R2} = +4.900V$  and  $V_{R3} = -0.400V$ .



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

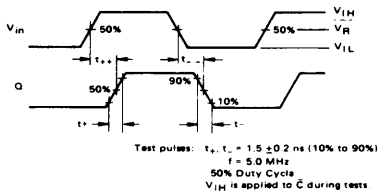
†Refer to Fig. 4 for input pulse definitions.

\* Complement of output under test should always be loaded with 50ohms to ground

Fig. 3 Switching time test circuit at +25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output



TEST PULSE LEVELS

	Pulse 1	Pulse 2	Pulse 3
$V_{IH}$	+2.100V	+5.000V	-0.300V
$V_R$	+2.000V	+4.900V	-0.400V
$V_{IL}$	+1.900V	+4.800V	-0.500V

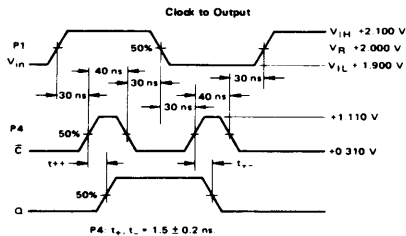


Fig. 4 Switching and propagation waveforms @ 25°C

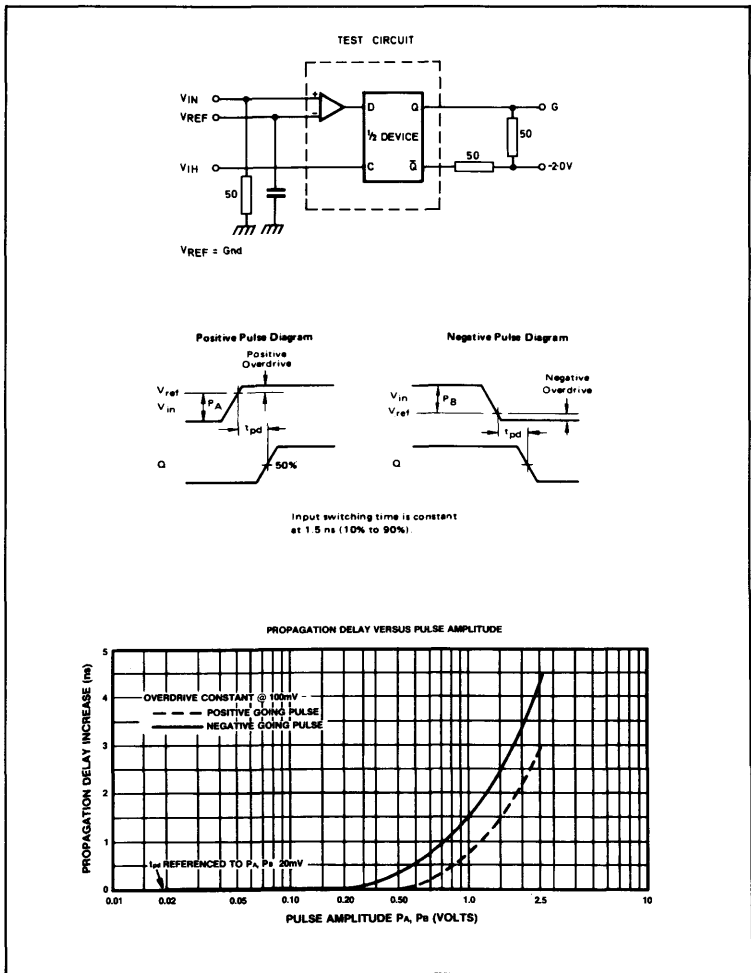


Fig. 5 Propagation delay ( $t_{pd}$ ) v. input pulse amplitude and constant overdrive

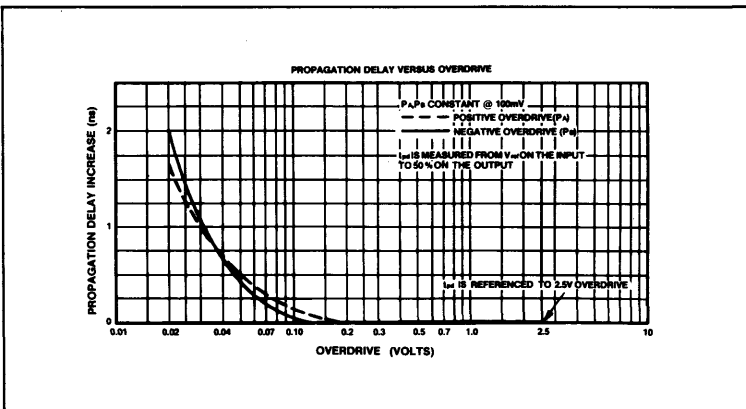


Fig. 5 (continued)

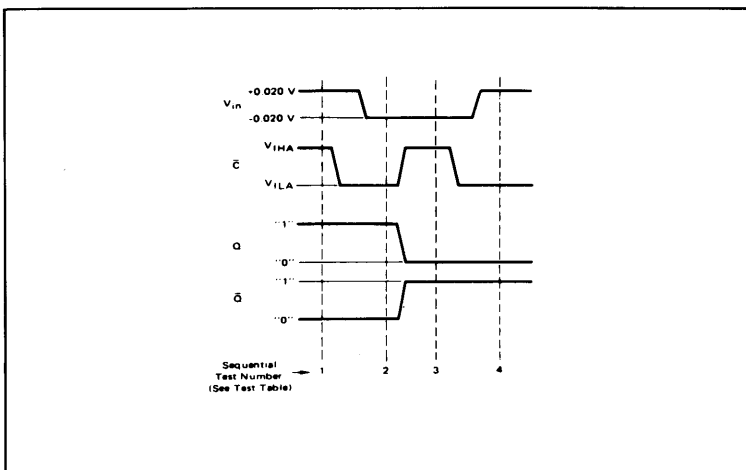


Fig. 6 Logic threshold tests (waveform sequence diagram)

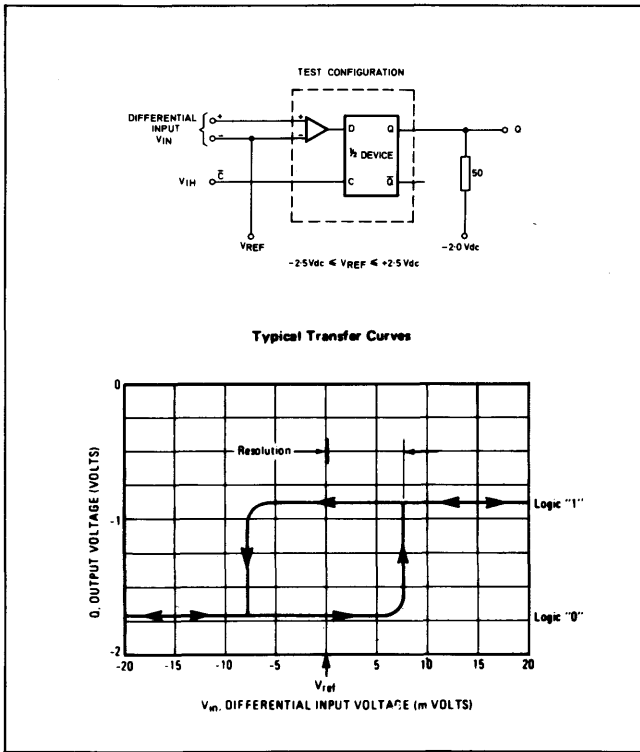


Fig. 7 Transfer characteristics (Q v. V<sub>in</sub>)

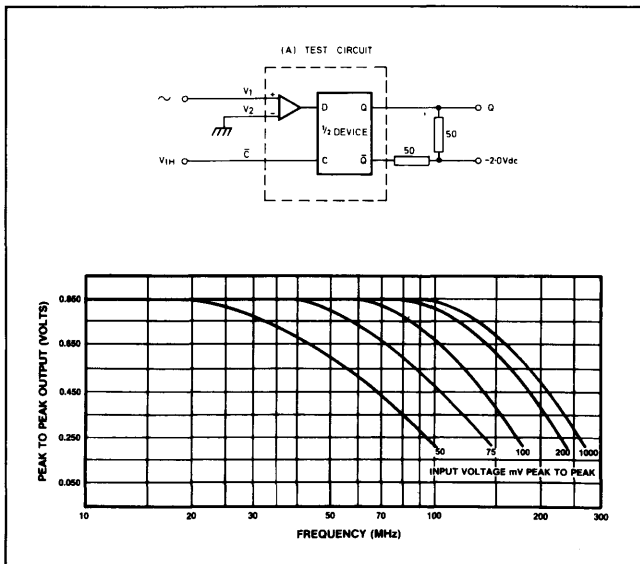


Fig. 8 Output voltage swing v. frequency

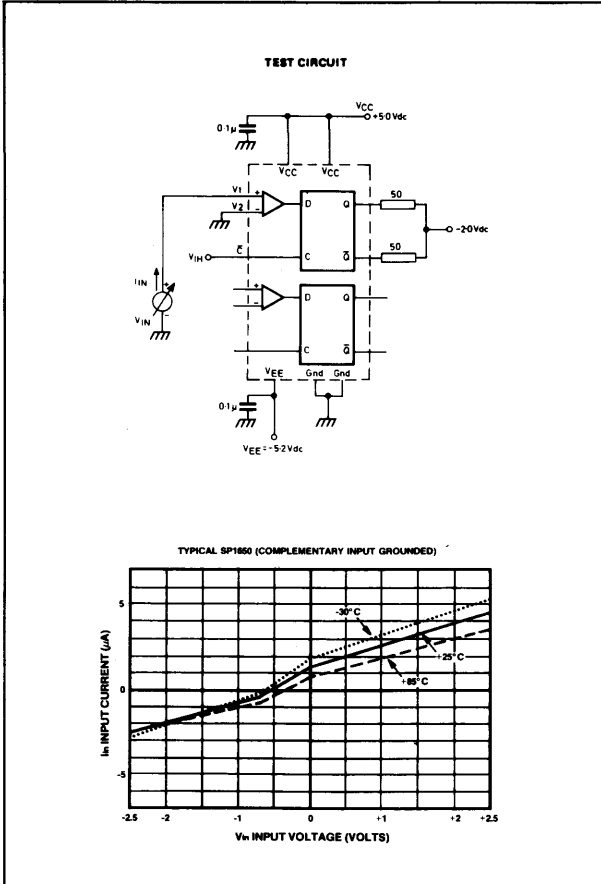
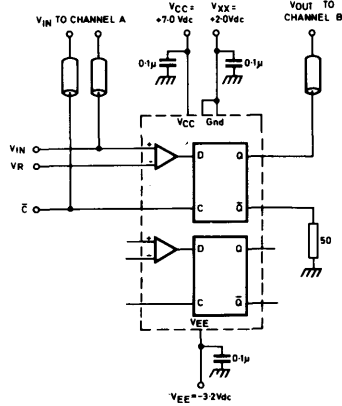


Fig. 9 Input current v. input voltage

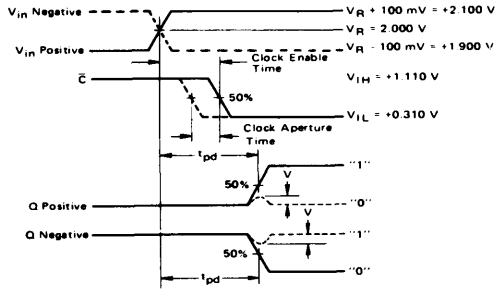




50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

**Analog Signal Positive and Negative Slew Case**



- Clock enable time=minimum time between analog and clock signal such that output switches, and  $t_{pd}$  (analog to Q) is not degraded by more than 200ps.
- Clock aperture time=time difference between clock enable time and time that output does not switch and V is less than 150 mV.

Fig. 10 Clock enable and aperture time test circuit and waveforms @ 25°C

# SP1658

## VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with ECL III and ECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in frequency modulation, phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

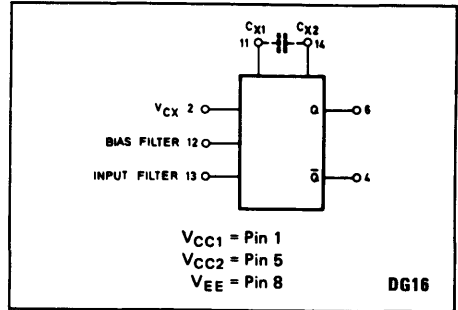


Fig. 1 Block diagram of SP1658

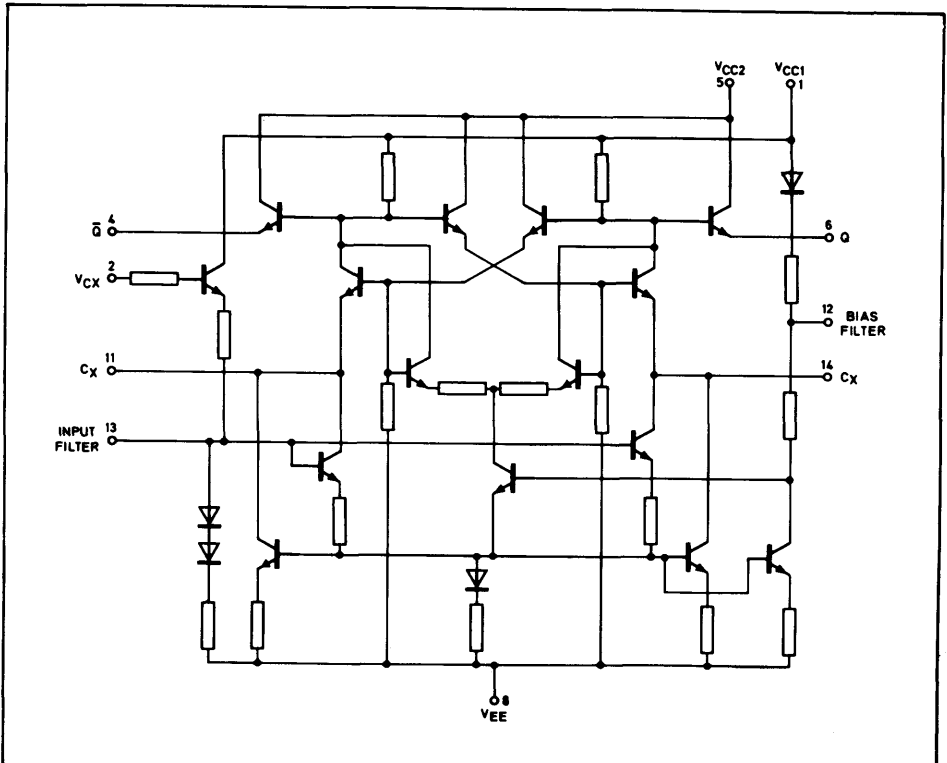


Fig. 2 Circuit diagram

**ELECTRICAL CHARACTERISTICS**

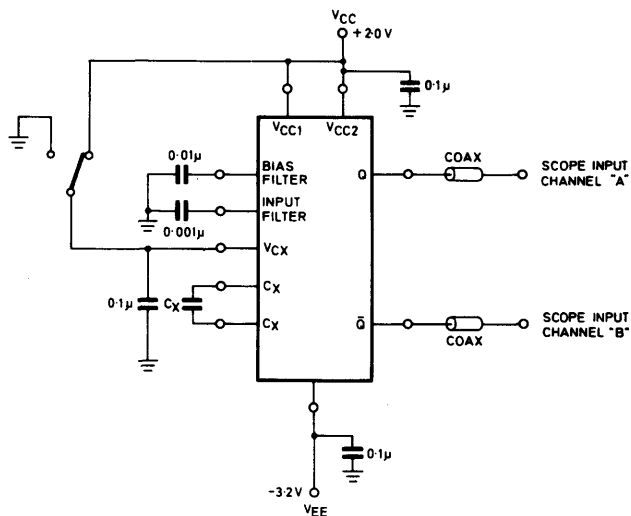
This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to  $-2.0$  volts.

Characteristic	Symbol	Pin Under Test	SP1658 Test Limits										TEST VOLTAGE VALUES				(VCC) Gnd
			-30°C		+25°C		+85°C		VOLTAGE APPLIED TO PINS LISTED BELOW				Vdc $\pm 1\%$				
			Min	Max	Min	Typ	Max	Min	Max	Unit	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>3</sub>	VEE			
Power Supply Drain Current	I <sub>E</sub>	8*	-	-	-	-	32	-	-	mAdc	2	-	8	1.5			
Input Current	I <sub>inH</sub>	2*	-	-	-	350	-	-	$\mu$ Adc	2	-	8	1.5				
Input Leakage Current	I <sub>inL</sub>	2*	-	-	-0.5	-	-	-	$\mu$ Adc	-	2	-	8	1.5			
High Output Voltage	V <sub>OH</sub>	4**	-1.045	-0.875	-0.960	-	-0.810	-0.890	Vdc	-	-	2	8	1.5			
Low Output Voltage	V <sub>OL</sub>	6*	-1.045	-0.875	-0.960	-	-0.810	-0.890	Vdc	-	-	2	8	1.5			
AC Characteristics (Figure 2)		4*	-1.890	-1.650	-1.850	-	-1.620	-1.830	Vdc	-	-	2	8	1.5			
(Tests shown for one output, but checked on both)		6*	-1.890	-1.650	-1.850	-	-1.620	-1.830	Vdc	-	-	2	8	1.5			
Rise Time (10% to 90%)	t <sub>r</sub>	6	-	3.6	-	-	3.5	-	ns	-	-	11,14	2	8	1.5		
Fall Time (10% to 90%)	t <sub>f</sub>	6	-	3.1	-	-	3.0	-	ns	-	-	11,14	2	8	1.5		
Oscillator Frequency	f <sub>osc1</sub> f <sub>osc2</sub>	-	130	-	130	155	190	110	MHz	-	-	11,14	2	8	1.5		
Tuning Ratio Test 1	f <sub>osc1</sub> f <sub>osc2</sub>	-	-	-	78	90	120	-	MHz	11,14	11,14	-	2	8	1.5		
		-	-	-	3.1	4.5	-	-	-	11,14	11,14	-	2	8	1.5		

① Test Temperature  
-30°C  
+25°C  
+85°C

\* Germanium diode (0.4 drop) forward biased from pin 11 to pin 14  
 \*\* Germanium diode (0.4 drop) forward biased from pin 14 to pin 11  
 † Tr - Output frequency at V<sub>CX</sub> = +2.0 V  
 ‡ Tr - Output frequency at V<sub>CX</sub> = Gnd

CX1 = 10pF connected from pin 11 to pin 14  
 CX2 = 5pF connected from pin 11 to pin 14



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be  $< \frac{1}{2}$  inch from  $TP_{in}$  to input pin and  $TP_{out}$  to output pin.

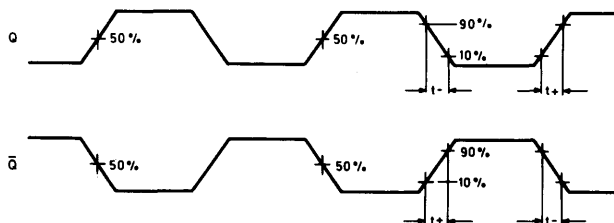


Fig. 3. Switching time test circuit and waveforms

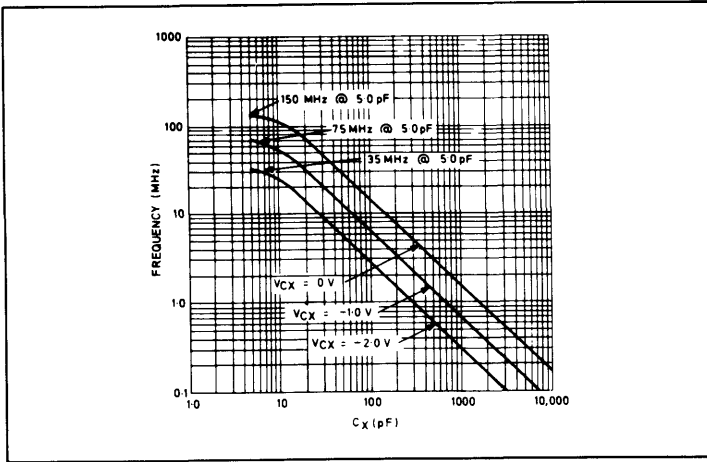


Fig.4 Output frequency v capacitance for three values of input voltage

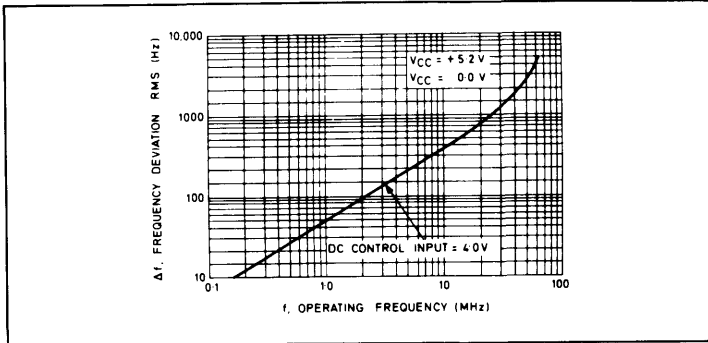


Fig.5 RMS noise deviation v operating frequency

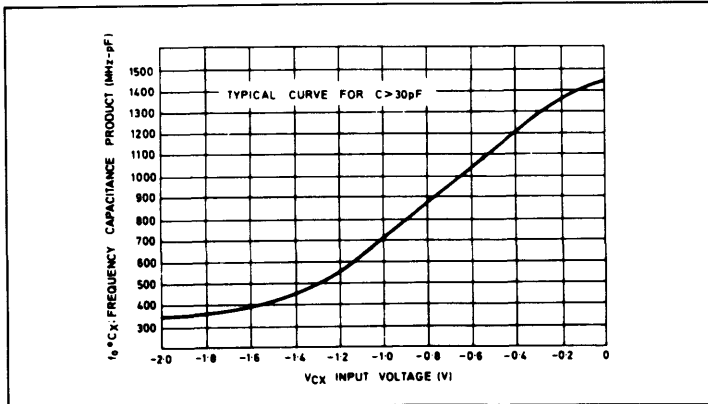


Fig.6 Frequency-capacitance product v control voltage  $V_{CX}$

# SP1660

## DUAL 4-INPUT OR/NOR GATE

SP1660 provides simultaneous OR-NOR output functions with the capability of driving 50 $\mu$ A lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (-30°C to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V<sub>EE</sub>.

### FEATURES

- Gate Switching Speed 1ns Typ.
- ECL 10000- Compatible
- 50 $\Omega$  Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

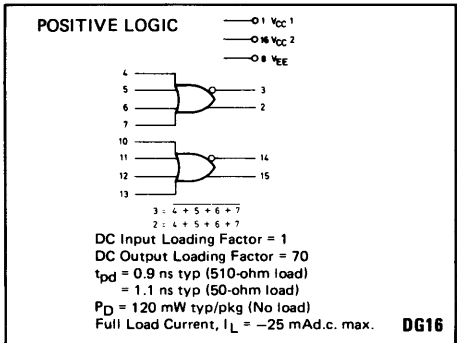


Fig. 1 Logic diagram

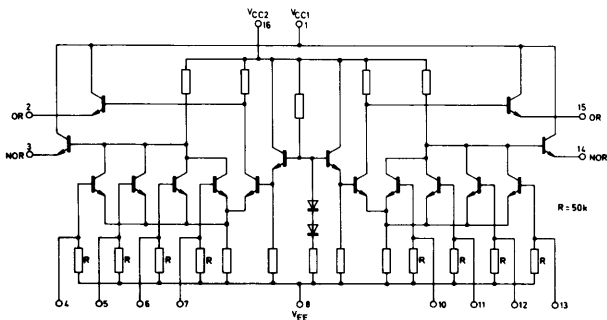


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to  $-2.0$  Vdc.

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits						Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					$(V_{CC})$ Gnd
			$-30^{\circ}\text{C}$		$+25^{\circ}\text{C}$		$+85^{\circ}\text{C}$			$V_{IHmax}$	$V_{ILmin}$	$V_{IHamin}$	$V_{ILAmax}$	$V_{EE}$	
			Min	Max	Min	Max	Min	Max		V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHamin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
Power Supply Drain Current	$I_E$	8	--	--	--	28	--	--	mAdc	--	--	--	8	1,16	
Input Current	$I_{inH}$	*	--	--	0.5	350	--	--	$\mu\text{Adc}$	*	*	--	8	1,16	
	$I_{inL}$	*	--	--	0.5	350	--	--	$\mu\text{Adc}$	*	*	--	8	1,16	
NOR Logic "1" Output Voltage	$V_{OH}$	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	--	4	--	8	1,16	
										5	--				
										6	--				
										7	--				
NOR Logic "0" Output Voltage	$V_{OL}$	3	-1.890	1.850	-1.850	-1.620	-1.830	-1.575	Vdc	4	--	--	8	1,16	
										5	--				
										6	--				
										7	--				
OR Logic "1" Output Voltage	$V_{OH}$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	--	--	8	1,16	
										5	--				
										6	--				
										7	--				
OR Logic "0" Output Voltage	$V_{OL}$	2	-1.890	-1.850	-1.850	-1.620	-1.830	-1.575	Vdc	--	4	--	8	1,16	
										5	--				
										6	--				
										7	--				
NOR Logic "1" Threshold Voltage	$V_{OHA}$	3	-1.065	--	-0.980	--	-0.910	--	Vdc	--	--	4	8	1,16	
												5			
												6			
												7			
NOR Logic "0" Threshold Voltage	$V_{OLA}$	3	--	-1.630	--	-1.600	--	-1.555	Vdc	--	--	4	8	1,16	
												5			
												6			
												7			
OR Logic "1" Threshold Voltage	$V_{OHA}$	2	-1.065	--	-0.980	--	-0.910	--	Vdc	--	--	4	8	1,16	
												5			
												6			
												7			
OR Logic "0" Threshold Voltage	$V_{OLA}$	2	--	-1.630	--	-1.600	--	-1.555	Vdc	--	--	4	8	1,16	
												5			
												6			
												7			
Switching Times (50 $\Omega$ Load)										Pulse In	Pulse Out		-3.2 V	+2.0 V	
Propagation Delay	$t_{4-3}$	3	--	1.8	--	1.7	--	1.9	ns	4	3	--	8	1,16	
	$t_{4-2}$	2	--	1.8	--	1.7	--	1.9		2	2	--			
	$t_{4-2+}$	2	--	1.6	--	1.5	--	1.7		3	2	--			
	$t_{4-3+}$	3	--	1.6	--	1.5	--	1.7		2	3	--			
Rise Time	$t_{3+}$	3	--	2.2	--	2.1	--	2.3	ns	4	3	--	8	1,16	
	$t_{2+}$	2	--	2.2	--	2.1	--	2.3		4	2	--			
Fall Time	$t_{3-}$	3	--	2.2	--	2.1	--	2.3	ns	4	3	--	8	1,16	
	$t_{2-}$	2	--	2.2	--	2.1	--	2.3		4	2	--			

\*Individually test each input applying  $V_{IH}$  or  $V_{IL}$  to the input under test.

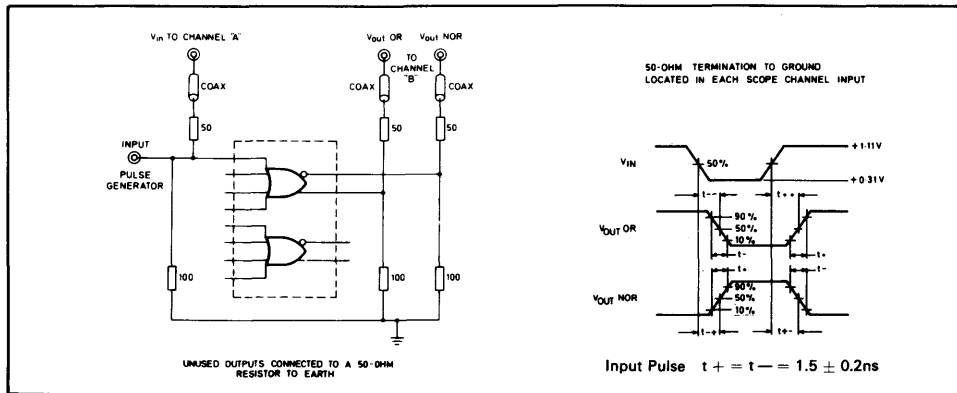


Fig. 3 Switching time test circuit and wave forms at  $+25^{\circ}\text{C}$

# SP1670

## MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pull-down resistors eliminate the need to tie unused inputs to V<sub>EE</sub>.

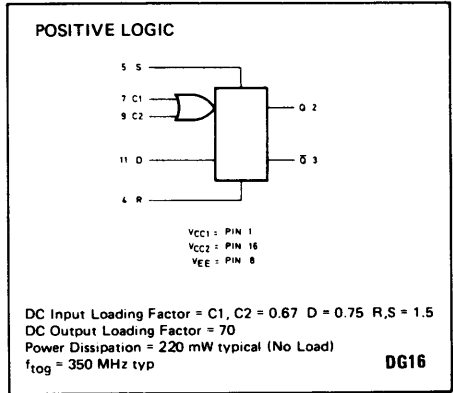


Fig. 1 Logic diagram

### FEATURES

- Toggle Frequency > 300 MHz
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

TRUTH TABLE				
R	S	D	C	Q <sub>n+1</sub>
L	H	φ	φ	H
H	L	φ	φ	L
H	H	φ	φ	N.D.
L	L	L	L	Q <sub>n</sub>
L	L	L	L	L
L	L	L	H	Q <sub>n</sub>
L	L	H	L	Q <sub>n</sub>
L	L	H	H	H
L	L	H	H	Q <sub>n</sub>

φ = Don't Care  
ND = Not Defined  
C = C1 + C2

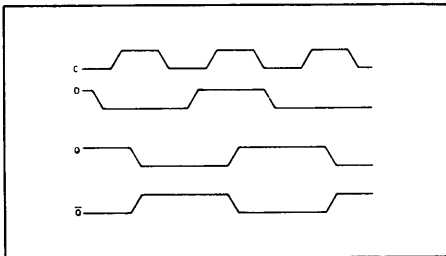


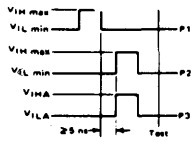
Fig. 2 Timing diagram



ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts.

Characteristic	Symbol	Pin Under Test	SP1670 Test Limits						Unit	TEST VOLTAGE VALUES (Volts)					P1	P2	P3	(V <sub>CC</sub> ) Gnd		
			-30°C		-25°C		-95°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>VLA</sub> max	V <sub>EE</sub>						
			Min	Max	Min	Max	Min	Max		-0.875	-1.890	-1.180	-1.515	-5.2						
			Min	Max	Min	Max	Min	Max		-0.810	-1.850	-1.095	-1.485	-5.2						
Power Supply Drain	I <sub>E</sub>	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1,16		
Input Current	I <sub>in H</sub>	4	—	—	—	—	—	—	4	—	—	—	—	8	—	—	—	1,16		
		5	—	—	—	550	—	—	5	—	—	—	—	—	—	—	—	—		
		9	—	—	—	250	—	—	9	—	—	—	—	—	—	—	—	—		
		7	—	—	—	250	—	—	7	—	—	—	—	—	—	—	—	—		
	I <sub>in L</sub>	4	—	—	0.5	—	—	—	—	9	4	—	—	—	8	—	—	—	1,16	
		5	—	—	—	—	—	—	—	9	5	—	—	—	—	—	—	—	—	
		9	—	—	—	—	—	—	—	7	9	—	—	—	—	—	—	—	—	
		7	—	—	—	—	—	—	—	9	7	—	—	—	—	—	—	—	—	
Logic "1" Output Voltage	V <sub>OH</sub>	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	vdc	—	4,7,11	—	—	—	8	9	5	—	1,16	
Logic "0" Output Voltage	V <sub>OL</sub>	2	-1.890	-1.850	-1.850	-1.670	-1.830	-1.575	vdc	11	5,7	—	—	—	8	9	4	—	1,16	
		3	—	—	—	—	—	—	—	—	4,9,11	—	—	—	—	7	5	—	—	
		3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	5	9	—	—
Logic "1" Threshold Voltage	V <sub>OH</sub> A	2	-1.065	—	-0.980	—	-0.910	—	vdc	—	4,7,11	—	—	—	8	9	—	5	1,16	
		3	—	—	—	—	—	—	—	—	—	—	—	—	—	7	—	—	—	
		2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	4	—	—	—
		3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	5	—	—	—
Logic "0" Threshold Voltage	V <sub>OL</sub> A	2	—	-1.630	—	-1.600	—	-1.555	vdc	11	5,7	—	—	—	8	9	—	4	1,16	
		3	—	—	—	—	—	—	—	—	—	—	—	—	—	7	—	—	—	
		2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	5	—	—	—
		3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	4	—	—	—
Switching Parameters	Clock to Output Delay (See Figure 1)	19+2+	9,2	—	—	—	—	—	ns	—	—	—	—	—	—	—	—	—	—	
		19+2-	9,2	1.0	2.7	1.1	2.5	1.1	2.9	—	—	—	—	—	—	—	—	—	—	—
		19+3+	9,3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		19+3-	9,3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Set to Output Delay (See Figure 2)	15+2+	5,2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		15+3-	5,3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Reset to Output Delay (See Figure 2)	14+2-	4,2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		14+3+	4,3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	Output	Rise Time	12+,13+	2,3	0.9	2.7	1.0	2.5	1.0	2.9	—	—	—	—	—	—	—	—	—	—
		Fall Time	12-,13-	2,3	0.5	2.1	0.6	1.9	0.6	2.3	—	—	—	—	—	—	—	—	—	—
	Set Up Time (See Figure 3)	11/11+	2	—	—	—	0.4	—	—	—	—	—	—	—	—	—	—	—	—	—
		14/10+	2	—	—	—	0.3	—	—	—	—	—	—	—	—	—	—	—	—	—
Hold Time (See Figure 3)	14/11+	2	—	—	—	0.5	—	—	—	—	—	—	—	—	—	—	—	—	—	
	14/10+	2	—	—	—	0.5	—	—	—	—	—	—	—	—	—	—	—	—	—	
Toggle Frequency (See Figure 4)	f <sub>tog</sub>	2	270	—	300	—	270	—	MHz	—	—	—	—	—	—	—	—	—	—	



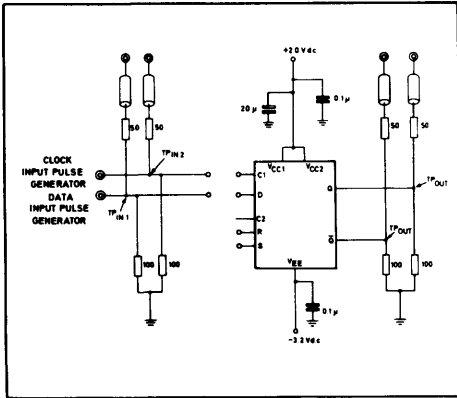


Fig. 3 Propagation delay test circuit

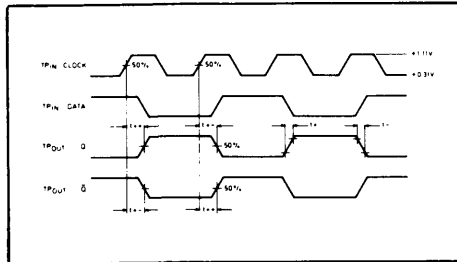


Fig. 4 Clock delay waveforms at +25°C

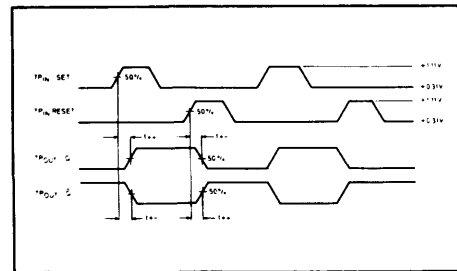
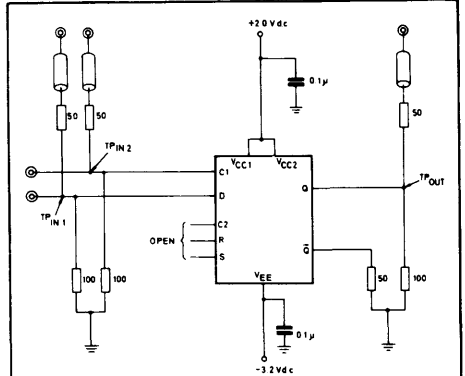
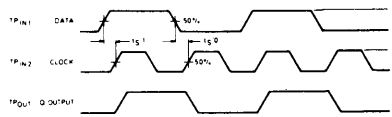


Fig. 5 Set/reset delay waveform at +25°C

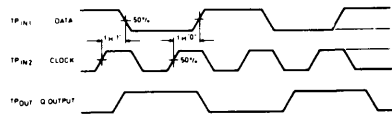


ALL INPUT AND OUTPUT CABLES TO THE SCOPE ARE EQUAL LENGTHS OF 50-OHM COAXIAL CABLE

Set-up and hold time test circuit



Set-up time waveforms at +25°C



Hold time waveforms at +25°C

Fig. 6 Set-up and hold time test circuit

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

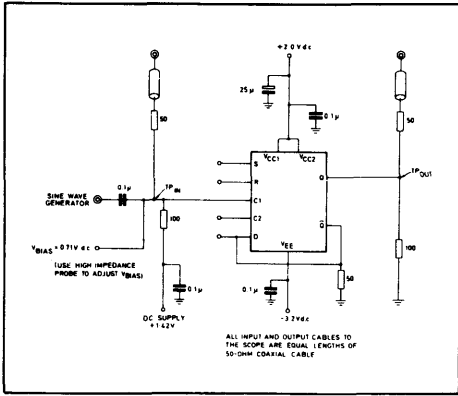


Fig. 7 Toggle frequency test circuit

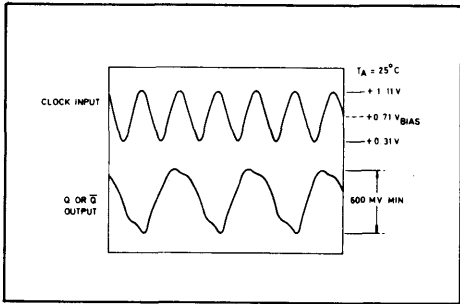


Fig. 8 Toggle frequency waveforms

The maximum toggle frequency of the SP1670 has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600mV
- OR
2. The device ceases to toggle (divide by two).  $V_{Bias}$  is defined by the test circuit Fig. 7 and by the waveform in Fig. 8.

Temperature	-30°C	+25°C	+85°C
$V_{Bias}$	+0.660V	+0.710V	+0.765V

Table 1 Variation of  $V_{Bias}$  with temperature

Figures 9 and 10 illustrate minimum clock pulse width recommended for reliable operation of the SP1670

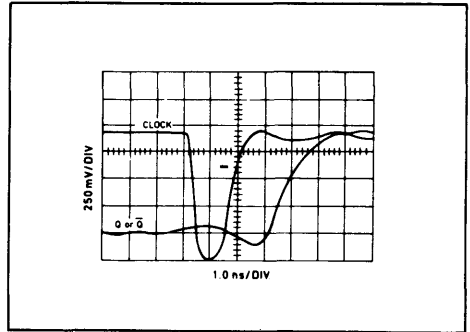


Fig. 9 Minimum 'down time' to clock (Output load = 50Ω)

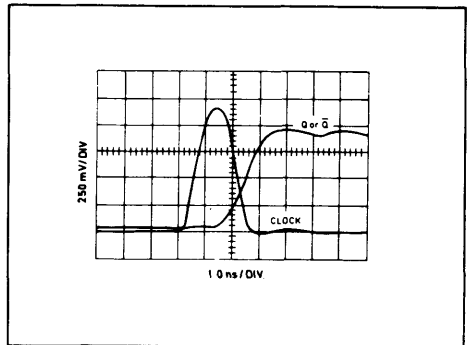


Fig. 10 Minimum 'up time' to clock (Output load = 50Ω)

**Operation of the Master-Slave Type D Flip-Flop**

In the circuit of Figure 11 assume that initially Q, C, R, S and D are at 0 levels and that  $\bar{Q}$  is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7, and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore

the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turns on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the  $\bar{Q}$  output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

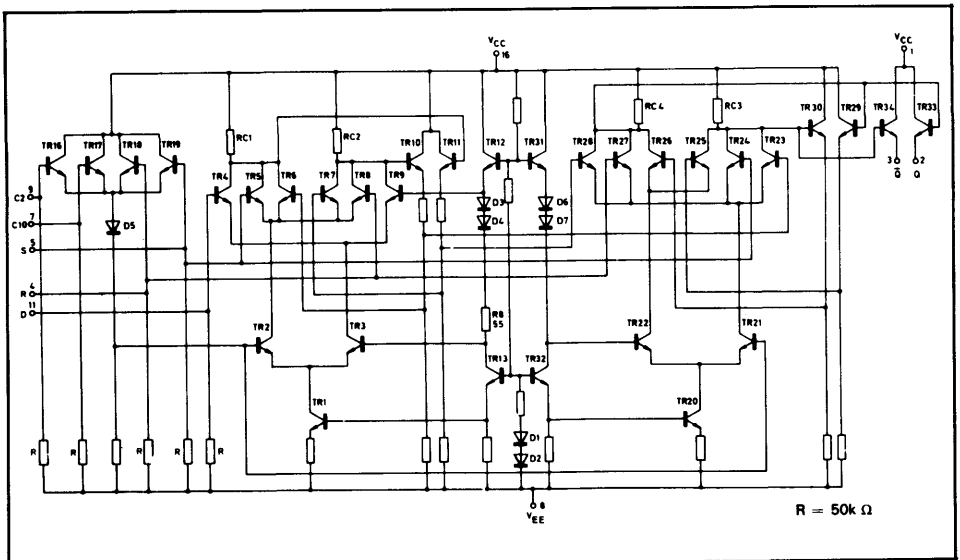


Fig. 11 SP1670 Circuit diagram





# SP16F60

## DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to VEE.

### FEATURES

- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible with SP1660

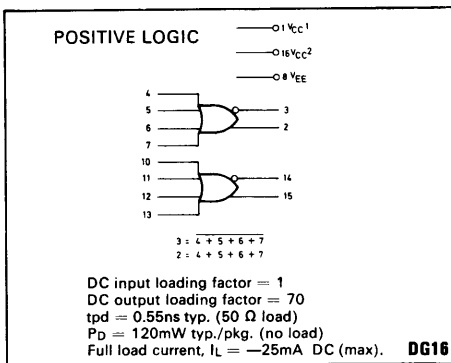


Fig. 1 Logic diagram

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

### ABSOLUTE MAXIMUM RATINGS

Power supply voltage | V<sub>CC</sub> - V<sub>EE</sub> | 8V  
 Base input voltage OV to V<sub>EE</sub>  
 O/P source current < 40mA  
 Storage temperature -55°C to +150°C  
 Junction operating temperature < +125°C

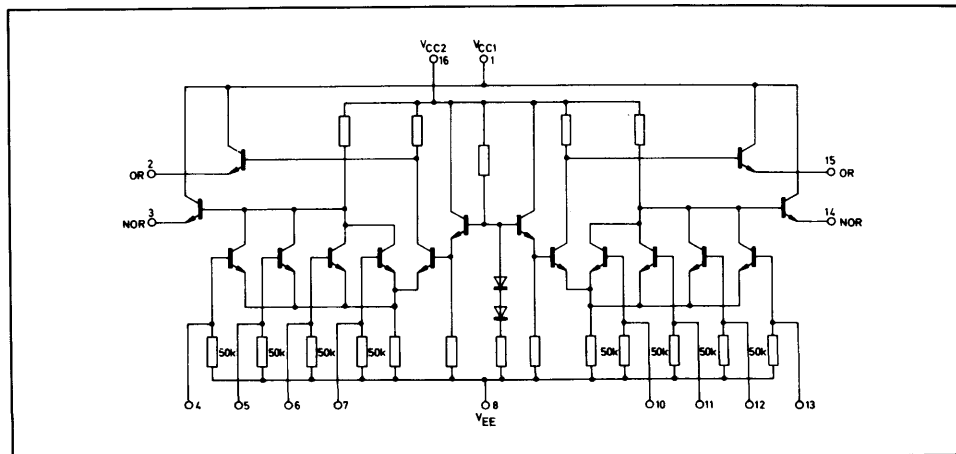


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc.

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits						Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					V <sub>CC</sub> (Gnd)
			-30°C		+25°C		+85°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>IHA</sub> max	V <sub>EE</sub>	
			Min	Max	Min	Max	Min	Max							
			TEST VOLTAGE VALUES (V)												
Power Supply Drain Current	I <sub>E</sub>	8	-	-	-	-	28	-	-	-	-	8	1.16		
Input Current	I <sub>IN</sub> H	*	-	-	-	-	350	-	-	-	-	8	1.16		
	I <sub>IN</sub> L	*	-	-	0.5	-	-	-	-	-	-	8	1.16		
NOR Logic 1 Output Voltage	V <sub>OH</sub>	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	-	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	4	5	6	7	↓	
NOR Logic 0 Output Voltage	V <sub>OL</sub>	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	-	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	5	6	7	↓		
OR Logic 1 Output Voltage	V <sub>OH</sub>	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	-	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	5	6	7	↓		
OR Logic 0 Output Voltage	V <sub>OL</sub>	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	-	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	5	6	7	↓		
NOR Logic 1 Threshold Voltage	V <sub>OHA</sub>	3	-1.065	-	-0.980	-	-0.910	-	V	-	-	-	4	8	1.16
		↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	5	6	7
NOR Logic 0 Threshold Voltage	V <sub>OLA</sub>	3	-	-1.630	-	-1.600	-	-1.555	V	-	-	-	4	8	1.16
		↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	5	6	7
OR Logic 1 Threshold Voltage	V <sub>OHA</sub>	2	-1.065	-	-0.980	-	-0.910	-	V	-	-	-	4	8	1.16
		↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	5	6	7
OR Logic 0 Threshold Voltage	V <sub>OLA</sub>	2	-	-1.630	-	-1.600	-	-1.555	V	-	-	-	4	8	1.16
		↓	↓	↓	↓	↓	↓	↓	↓	-	-	-	5	6	7
Switching Times (50Ω Load) Propagation Delay	t <sub>4-3</sub> , t <sub>4-2</sub> , t <sub>4+2</sub> , t <sub>4-3</sub>	3	Typ	Max	Typ	Max	Typ	Max	ns	Pulse In	Pulse Out	-	-3.2V	+2.0V	
		↓	↓	↓	↓	↓	↓	↓	↓	4	2	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	↓	3	2	-	8	1.16
		↓	↓	↓	↓	↓	↓	↓	↓	↓	2	3	-	8	1.16
Rise Time 20% to 80%	t <sub>3+</sub> , t <sub>2+</sub>	3	-	-	0.4	0.6	-	-	ns	4	3	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	4	2	-	8	1.16	
Fall Time 20% to 80%	t <sub>3-</sub> , t <sub>2-</sub>	3	-	-	0.4	0.6	-	-	ns	4	3	-	8	1.16	
		↓	↓	↓	↓	↓	↓	↓	↓	4	2	-	8	1.16	

\* Individually test each input applying V<sub>IH</sub> or V<sub>IL</sub> to the input under test.

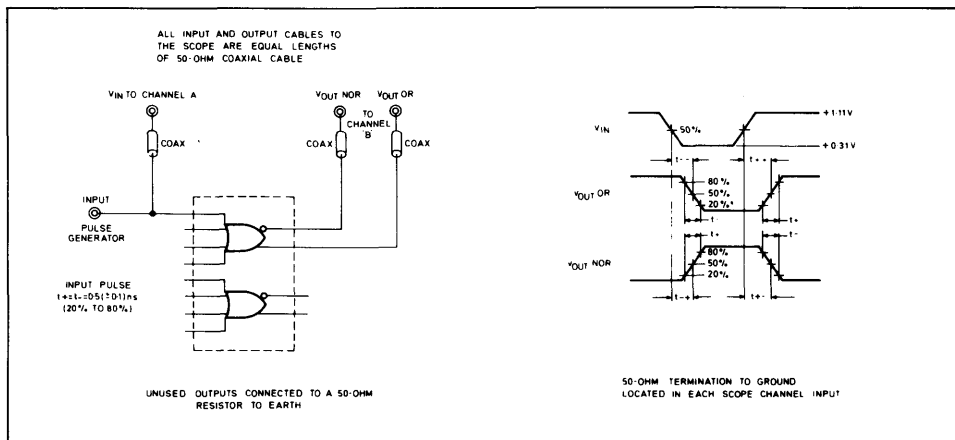


Fig. 3 Switching time test circuit and waveforms at +25°C

# SP16F70

## MASTER/SLAVE D TYPE FLIP-FLOP

The SP16F70 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP16F70 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V<sub>EE</sub>.

### FEATURES

- Toggle Frequency >350MHz
- ECL 10000 Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

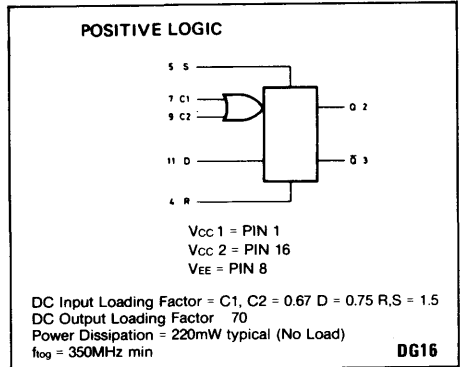


Fig. 1 Logic diagram

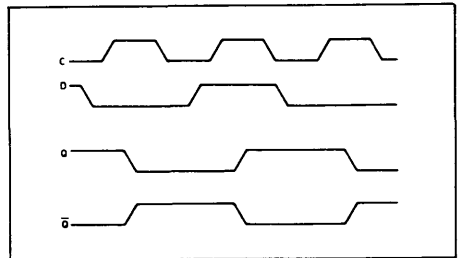


Fig. 2 Timing diagram

TRUTH TABLE				
R	S	D	C	Q <sub>n+1</sub>
L	H	φ	φ	H
H	L	φ	φ	L
H	H	φ	φ	N.D.
L	L	L	L	Q <sub>n</sub>
L	L	L	↗	L
L	L	L	H	Q <sub>n</sub>
L	L	H	L	Q <sub>n</sub>
L	L	H	↗	H
L	L	H	H	Q <sub>n</sub>

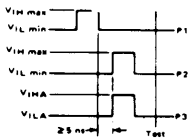
φ = Don't Care  
ND = Not Defined  
C = C1 + C2



ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts.

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE VALUES (Volts)										P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	(V <sub>CC</sub> ) Gnd						
			-30°C		-25°C		-85°C		V <sub>IH</sub> max		V <sub>IL</sub> min						V <sub>IHA</sub> min		V <sub>IHA</sub> max		V <sub>EE</sub>	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max					Min	Max	Min	Max	Min	Max
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW:														V <sub>IH</sub> max		V <sub>IL</sub> min		V <sub>IHA</sub> min	
Power Supply Drain	I <sub>C</sub>	8	—	—	—	48	—	—	—	mADC	7.9	—	—	—	—	8	—	—	—	1.16		
Input Current	I <sub>in</sub>	4	—	—	—	550	—	—	—	μADC	4	—	—	—	—	8	—	—	—	1.16		
		5	—	—	—	550	—	—	—	—	5	—	—	—	—	—	—	—	—	—		
		9	—	—	—	250	—	—	—	—	9	—	—	—	—	—	—	—	—	—		
		7	—	—	—	250	—	—	—	—	7	—	—	—	—	—	—	—	—	—		
		11	—	—	—	270	—	—	—	—	11	—	—	—	—	—	—	—	—	—		
		4	—	—	0.5	—	—	—	—	—	μADC	9	4	—	—	—	8	—	—	—	1.16	
		5	—	—	—	—	—	—	—	—	—	9	5	—	—	—	—	—	—	—	—	
9	—	—	—	—	—	—	—	—	—	7	9	—	—	—	—	—	—	—	—			
7	—	—	—	—	—	—	—	—	—	9	7	—	—	—	—	—	—	—	—			
11	—	—	—	—	—	—	—	—	—	9	11	—	—	—	—	—	—	—	—			
Logic "1" Output Voltage	V <sub>OH</sub>	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	vdc	—	4,7,11	—	—	—	8	9	5	—	1,16			
3	—	—	—	—	—	—	—	—	—	11	5,9	—	—	—	7	4	—	—	—			
3	—	—	—	—	—	—	—	—	—	11	5,7	—	—	—	4	9	—	—	—			
3	—	—	—	—	—	—	—	—	—	11	4,9,11	—	—	—	4	9	—	—	—			
Logic "0" Output Voltage	V <sub>OL</sub>	2	-1.890	-1.850	-1.850	-1.620	-1.830	-1.575	vdc	—	11	5,7	—	—	8	9	4	—	1,16			
3	—	—	—	—	—	—	—	—	—	—	4,9,11	—	—	—	7	5	—	—	—			
2	—	—	—	—	—	—	—	—	—	—	4,9,11	—	—	—	5	9	—	—	—			
2	—	—	—	—	—	—	—	—	—	—	11	5,9	—	—	4	7	—	—	—			
Logic "1" Threshold Voltage	V <sub>OH</sub> A	2	-1.065	—	-0.980	—	-0.910	—	vdc	—	4,7,11	—	—	—	8	9	—	5	1,16			
3	—	—	—	—	—	—	—	—	—	11	5,9	—	—	—	7	—	4	—	—			
3	—	—	—	—	—	—	—	—	—	11	5,7	—	—	—	4	9	—	—	—			
3	—	—	—	—	—	—	—	—	—	—	4,9,11	—	—	—	4	5	—	—	—			
2	—	—	—	—	—	—	—	—	—	—	5,7	11	—	—	4	9	—	—	—			
3	—	—	—	—	—	—	—	—	—	—	4,9	—	—	—	5	7	—	—	—			
Logic "0" Threshold Voltage	V <sub>OL</sub> A	2	—	-1.630	—	-1.600	—	-1.555	vdc	—	11	5,7	—	—	8	9	—	4	1,16			
3	—	—	—	—	—	—	—	—	—	—	4,9,11	—	—	—	7	—	5	—	—			
3	—	—	—	—	—	—	—	—	—	—	11	5,7	—	—	4	—	9	—	—			
3	—	—	—	—	—	—	—	—	—	—	4,9,11	—	—	—	5	—	7	—	—			
3	—	—	—	—	—	—	—	—	—	—	11	5,9	—	—	4	—	7	—	—			
3	—	—	—	—	—	—	—	—	—	—	4,7	—	—	—	5	9	—	—	—			
3	—	—	—	—	—	—	—	—	—	—	5,9	11	—	—	4	7	—	—	—			
Switching Parameters			Min	Max	Min	Max	Min	Max							-3.2 Vdc				-2.0 Vdc			
Clock to Output Delay	19+2+4	9.2	1.0	2.7	1.1	2.5	1.1	2.4	ns	—	—	—	—	—	8	—	—	—	1.16			
	19+2	9.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
	19+3+4	9.3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
	19+3	9.3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
	15+2	5.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
	15+3	5.3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
	14+2	4.2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
	14+3	4.3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
Output																						
Rise Time	12+13+	2.3	0.9	2.7	1.0	2.5	1.0	2.9	—	—	—	—	—	—	—	—	—	—	—			
Fall Time	12-13-	2.3	0.5	2.1	0.6	1.9	0.6	2.3	—	—	—	—	—	—	—	—	—	—	—			
Set Up Time	1 <sup>1</sup> / <sub>2</sub> 1 <sup>1</sup> / <sub>2</sub>	2	—	—	—	0.4	—	—	—	—	6	—	—	—	—	—	—	—	—			
	1 <sup>1</sup> / <sub>2</sub> 0 <sup>1</sup> / <sub>2</sub>	2	—	—	—	0.5	—	—	—	—	6	—	—	—	—	—	—	—	—			
	14 <sup>1</sup> / <sub>2</sub> 1 <sup>1</sup> / <sub>2</sub>	2	—	—	—	0.3	—	—	—	—	6	—	—	—	—	—	—	—	—			
	14 <sup>1</sup> / <sub>2</sub> 0 <sup>1</sup> / <sub>2</sub>	2	—	—	—	0.5	—	—	—	—	6	—	—	—	—	—	—	—	—			
Toggle Frequency	f <sub>top</sub>	2	350	—	350	—	350	—	MHz	—	—	—	—	—	—	—	—	—	—			



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# SP9131

## 520MHz ECL DUAL D FLIP-FLOP

The SP9131 Dual D type flip-flop is pin compatible with 10131, but has improved dynamic performance.

### FEATURES

- Guaranteed Operation at 520MHz
- Separate or Common Clock
- Independent Set and Reset Inputs
- Master Slave Operation
- -5.2V Supply
- Operating Temperature Range -30°C to +85°C
- ECL 10K Compatible
- Pin Compatible with MC10131/102131/105131 - But Faster

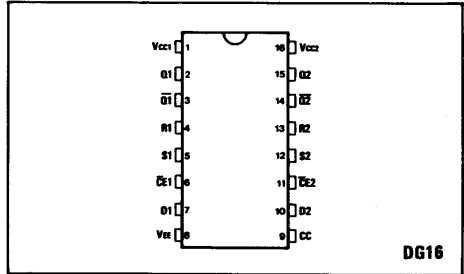


Fig.1 Pin connections - top view

### R-S TRUTH TABLE

R	S	Q <sub>n</sub> + 1
L	L	Q <sub>n</sub>
L	H	H
H	L	L
H	H	ND

### CLOCKED TRUTH TABLE

C	D	Q <sub>n</sub> + 1
L	X	Q <sub>n</sub>
H	L	L
H	H	H

X = Don't care

C = CE + CC

A clock H is a clock transition from a low to a high state.

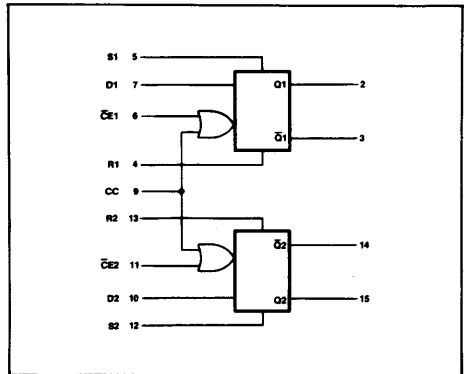


Fig.2 SP9131 logic diagram

### ABSOLUTE MAXIMUM RATINGS

Power supply voltage	V <sub>CC</sub> - V <sub>EE</sub>   8V
Base input voltage	0V to V <sub>EE</sub>
Output source current	< 40mA
Storage temperature	-55°C to +150°C
Junction operating temperature	< +125°C

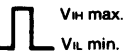
**ELECTRICAL CHARACTERISTICS**

The SP9131 circuit has been designed to meet the DC specifications shown in the test table after the circuit equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

Characteristic	Symbol	Pin under test	Test limits						TEST VOLTAGES (V)											
			-30°C		+25°C		+85°C		V <sub>in</sub> Min.		V <sub>in</sub> Max.		V <sub>in</sub> Min.		V <sub>in</sub> Max.					
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.					
Power supply current Input current	I <sub>E</sub>	8	-	95	70	87	-	95	mA	-	-	-	-	-	-	-	-	-	-	-
	I <sub>INH</sub>	4	-	-	-	600	-	-	μA	4	-	-	-	-	-	-	-	-	-	-
Input leakage current	I <sub>inL</sub>	5	-	-	-	300	-	-	-	5	-	-	-	-	-	-	-	-	-	-
		6	-	-	-	300	-	-	-	6	-	-	-	-	-	-	-	-	-	-
		7	-	-	-	300	-	-	-	7	-	-	-	-	-	-	-	-	-	-
		9	-	-	-	420	-	-	-	9	-	-	-	-	-	-	-	-	-	-
		4,5 (Note 1) 6,7,9	-	-	-	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Logic '1' output voltage	V <sub>OH</sub>	2	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	5	-	-	-	-	-	-	-	-	-
		2 (Note 2)	-1.06	-0.89	-0.96	0.81	-0.89	-0.70	V	7	-	-	-	-	-	-	-	-	-	-
Logic '0' output voltage	V <sub>OL</sub>	3	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	5	-	-	-	-	-	-	-	-	-
		3 (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	7	-	-	-	-	-	-	-	-	-
Logic '1' threshold voltage	V <sub>OH1</sub>	2	-1.08	-0.98	-	-	-0.91	-	-	V	-	-	-	-	-	-	-	-	-	-
		2 (Note 2)	-1.08	-0.98	-	-	-0.91	-	-	V	-	-	-	-	-	-	-	-	-	-
Logic '0' threshold voltage	V <sub>OL1</sub>	3	-	-1.655	-	-	-1.63	-	-	V	-	-	-	-	-	-	-	-	-	-
		3 (Note 2)	-	-1.655	-	-	-1.63	-	-	V	-	-	-	-	-	-	-	-	-	-
SWITCHING TIMES	Clock input propagation delay	t <sub>tr+2</sub>	0.5	1.8	0.5	1.0	1.8	0.6	2.1	ns	-	-	-	-	-	-	-	-	-	-
		t <sub>tr-2+</sub>	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Rise time (20 to 80 %) Fall time (20 to 80 %) Set input propagation delay	t <sub>r</sub>	2	0.5	1.5	0.5	1.0	1.5	0.5	1.6	ns	-	-	-	-	-	-	-	-	-	-
		2	0.4	1.4	0.4	1.4	0.5	1.5	0.5	2.3	ns	-	-	-	-	-	-	-	-	-
		2	0.5	2.0	0.5	1.0	2.0	0.6	2.3	-	-	-	-	-	-	-	-	-	-	-
		15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Reset input propagation delay	t <sub>tr-14</sub>	14	-	-	-	-	-	-	-	ns	-	-	-	-	-	-	-	-	-	-
		15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Setup time Hold time Toggle frequency (max.)	t <sub>su+14+15</sub> t <sub>ho+14</sub> f <sub>reg</sub>	14	-	-	-	-	-	-	-	ns	-	-	-	-	-	-	-	-	-	-
		14	-	-	-	-	-	-	-	-	ns	-	-	-	-	-	-	-	-	-
		14	-	-	-	-	-	-	-	-	ns	-	-	-	-	-	-	-	-	-
		7	1.0	1.0	1.0	-	1.0	1.0	0.2	500	MHz	-	-	-	-	-	-	-	-	-
		7	0.2	0.2	0.2	-	0.2	0.2	0.2	500	MHz	-	-	-	-	-	-	-	-	-

**NOTES**

1. Individually test each input, apply V<sub>in</sub> min to pin under test.
2. Output level to be measured after a clock pulse has been applied to the CE input (pin 6).





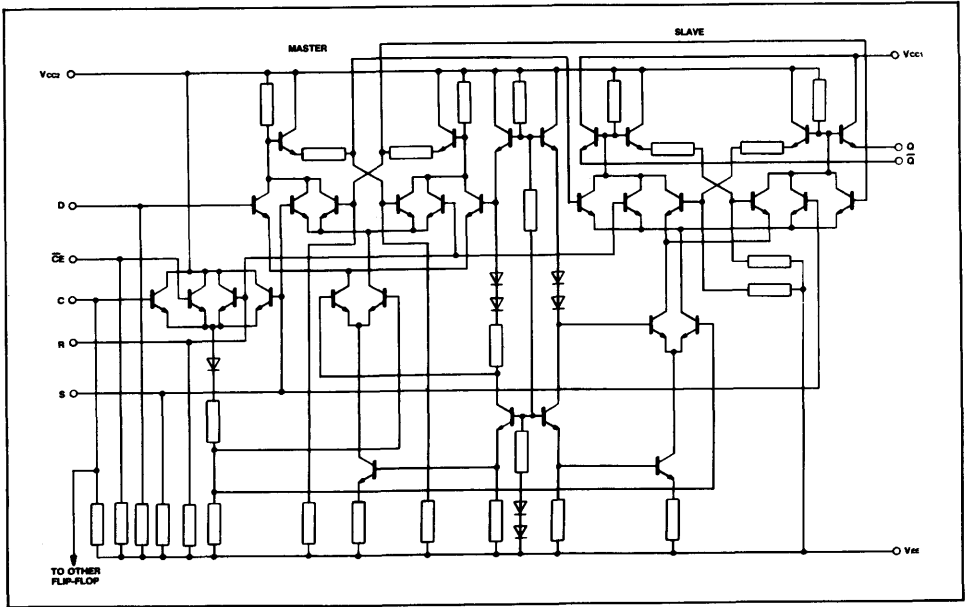


Fig.5 Circuit schematic (1/2 of circuit shown)

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# SP9210

## 200MHz 8-BIT LATCH

The SP9210 is a dual 4-bit master/slave D-type flip-flop with asynchronous set and reset which override the clock input.

Data is entered into the master when the clock is low and is transferred to the slave on the positive transition of the clock, the device being edge-sensitive.

On-chip pulldown resistors eliminate the need to tie unused inputs to V<sub>EE</sub>.

### FEATURES

- Dual 4-Bit Master/Slave D-Type Flip-Flop
- Clock Rate in Excess of 200MHz
- -5.2V Supply
- Current Consumption Typically 145mA
- Input Current Less Than 330µA
- Operating Temperature Range -30°C to +85°C
- Set and Reset Inputs Provided
- ECL 10K Compatible
- Dual Clock Inputs

### PIN NAMES

S1-4	Set input for 1-4
S5-8	Set input for 5-8
V <sub>EE</sub>	Supply voltage (-VE)
D1-8	Data inputs 1-8
CLK1-4	Clock latch for 1-4
CLK5-8	Clock latch for 5-8
Q1-8	Outputs latches 1-8
R1-4	Reset input latch for 1-4
R5-8	Reset input latch for 5-8

### R - S TRUTH TABLE

R	S	Q <sub>n</sub> + 1
L	L	Q <sub>n</sub>
L	H	H
H	L	L
H	H	ND

R = Reset, S = Set,  
ND = Not defined

### CLOCKED TRUTH TABLE

C	D	Q <sub>n</sub> + 1
L	X	Q <sub>n</sub>
↑	L	L
↑	H	H

C = Clock, D = Data,  
↑ = Rising edge, X = Don't care

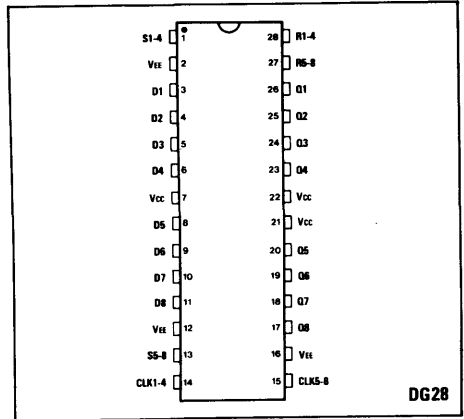


Fig.1 Pin connections - top view

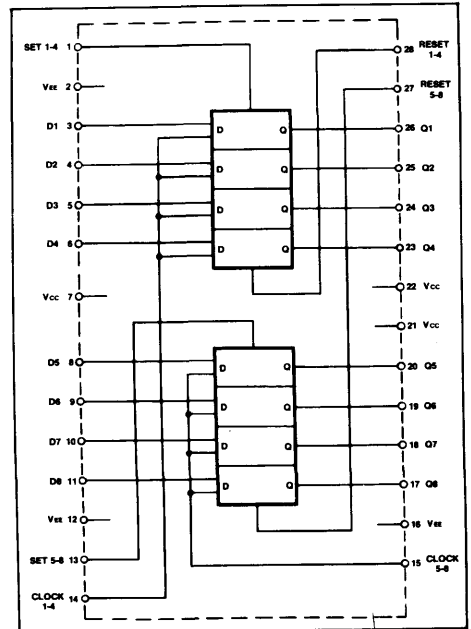


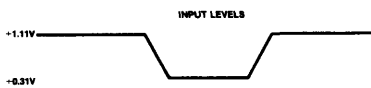
Fig.2 SP9210 block diagram

**ELECTRICAL CHARACTERISTICS**

Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

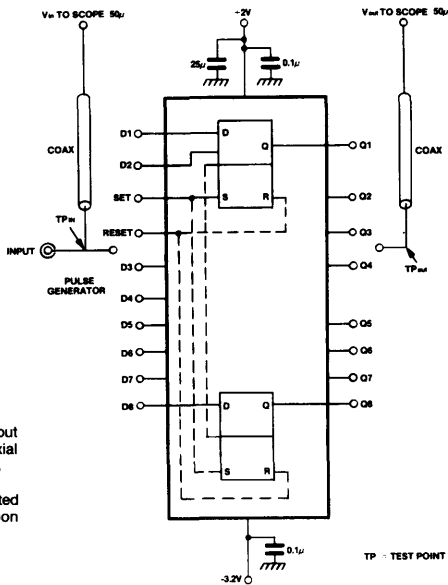
Characteristic	Symbol	Pin under test	-30°C		+25°C		+85°C		TEST VOLTAGES (V)					V <sub>cc</sub> (GND)		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	V <sub>H</sub> Max.	V <sub>L</sub> Min.	V <sub>HA</sub> Min.	V <sub>LA</sub> Max.		V <sub>IE</sub>	
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW									V <sub>H</sub> MAX.	V <sub>L</sub> MIN.		V <sub>HA</sub> MIN.	V <sub>LA</sub> MAX.
POWER SUPPLY Drain current Input current	I <sub>EE</sub>	2,12,16	-	200	-	145	180	-	200	mA	-	-	-	-	2,12,16	7,21,22
	I <sub>IN</sub>	Set/Reset Clock Data	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
Input leakage current Logic '1' output voltage	I <sub>INL</sub>	All inputs	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
	V <sub>OH</sub>	All outputs	-1.06	-0.89	0.5	-0.96	-	-0.89	-0.70	µA	Data inputs	-	-	-	2,12,16	7,21,22
Logic '0' output voltage	V <sub>OL</sub>	All outputs (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.615	-	V	Data inputs	-	-	-	2,12,16	7,21,22
Logic '1' threshold voltage	V <sub>OH1</sub>	All outputs (Note 2)	-1.08	-	-0.98	-	-	-0.91	-	V	Data inputs	-	-	-	2,12,16	7,21,22
Logic '0' threshold voltage	V <sub>OL0</sub>	All outputs (Note 2)	-	-1.655	-	-	-1.63	-	-1.595	V	Data inputs	-	-	-	2,12,16	7,21,22
SWITCHING TIMES Clock input propagation delay Rise time (20 % - 80 %) Fall time (20 % - 80 %) Set propagation delay Reset propagation delay Set up time Hold time Max. clock frequency	t <sub>a+</sub>	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	+1,11V Data inputs	-10,3V Clock inputs	Pulse out Outputs	-3,2V Pulse out Outputs	-2,0V 7,21,22	
	t <sub>a-</sub>	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	-	Data inputs	Clock Outputs	2,12,16 7,21,22		
	t <sub>r</sub>	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	Data inputs	Clock Outputs	Outputs	2,12,16 7,21,22		
	t <sub>f</sub>	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	-	Data inputs	Clock Outputs	Outputs	2,12,16 7,21,22	
	t <sub>set</sub>	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	Set inputs	Clock Outputs	Outputs	2,12,16 7,21,22	
	t <sub>reset</sub>	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	Reset inputs	Clock Outputs	Outputs	2,12,16 7,21,22	
	t <sub>s</sub>	Data inputs	1.5	-	1.5	-	-	-	1.5	-	ns	-	Data, Clock inputs	Clock Outputs	Outputs	2,12,16 7,21,22
	t <sub>h</sub>	Data inputs	1.0	-	1.0	-	-	-	1.0	-	ns	-	Data, Clock inputs	Clock Outputs	Outputs	2,12,16 7,21,22
	f <sub>CLK</sub>	All outputs	-	-	200	-	-	-	-	-	MHz	Data inputs	Clock inputs	Outputs	2,12,16 7,21,22	

NOTES  
 1. Each input, pin tested individually.  
 2. Output level to be measured after a clock pulse has been applied.

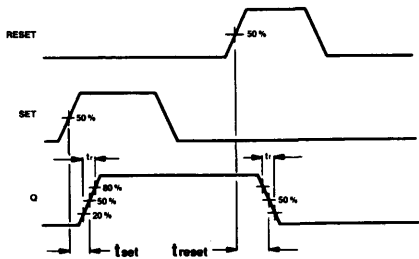


50 ohm to ground located in each scope channel input. All input and output cables to the scope are equal length of 50 ohm coaxial cable. Wire length should be  $\frac{1}{4}$  inch from TP<sub>IN</sub> to input pin and TP<sub>OUT</sub> to output pin.

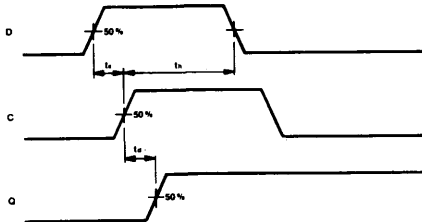
With supply voltages at 2V and -3.2V outputs should be terminated with 50 ohms to ground; this results in an output level translation giving V<sub>OH</sub> = 1.11V and V<sub>OL</sub> = +0.31V.



**SET AND RESET TIMING DIAGRAM**



**CLOCK AND DATA TIMING DIAGRAM**



**NOTE**

t<sub>setup</sub> is the minimum time before the positive transition of the clock pulse (C) that information must be present at data input (D).

t<sub>hold</sub> is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at data input (D).

Fig.3 Test circuit details for dynamic test



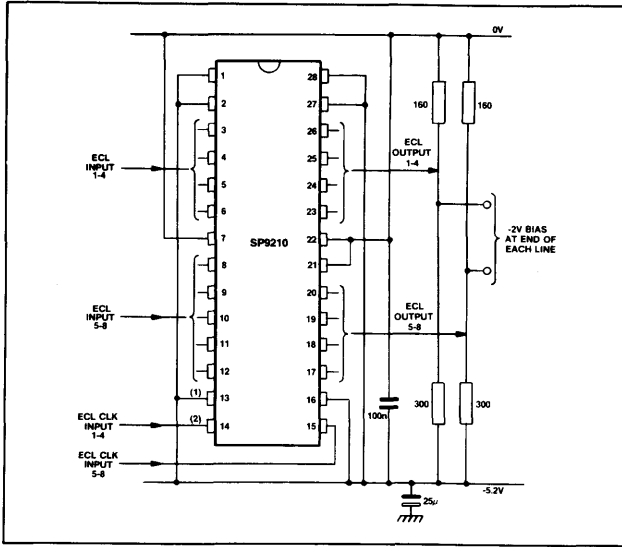


Fig.4 ECL 4 x 4 latch with 1000Ω output termination

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have 'pre-production' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of 'full production' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

# SP9215

## 10-BIT 50MHz ECL UP/DOWN COUNTER

The Plessey SP9215 is an ECL compatible 10-bit Synchronous UP/DOWN Counter capable of operating at clock frequencies in excess of 50MHz. The circuit is designed to operate in preset, hold, count up, and count down modes selected by two control inputs. A count enable input and terminal count output enable counters to be cascaded with no additional components. The terminal count output goes low when the counter reaches the all 'ones' state (count up) or the all 'zeros' state (count down). Outputs change state on the positive edge of the clock pulse.

The circuit operates from a -5.2 volt power supply and is packaged in 28-lead dual-in-line package.

Input pulldown resistors eliminate the need to tie unused inputs to  $V_{EE}$ .

### FEATURES

- Fully Synchronous
- Easily Cascadable
- Presettable for Programmable Applications
- Maximum Clock Frequency in Excess of 50MHz
- Power Consumption 800mW Typical
- Functionally Similar to F10136
- Operating Temperature Range -30°C to +85°C
- -5.2V Supply

### CONTROL TRUTH TABLE

$\overline{CE}$	S1	S2	Mode	$\overline{TC}$
X	L	L	Preset	H
L	L	H	Count Up	Note 1
L	H	L	Count Down	Note 1
X	H	H	Hold	H
H	L	H	Hold	H
H	H	L	Hold	H

### NOTE

$\overline{TC}$  is normally High and goes Low on the terminal count.

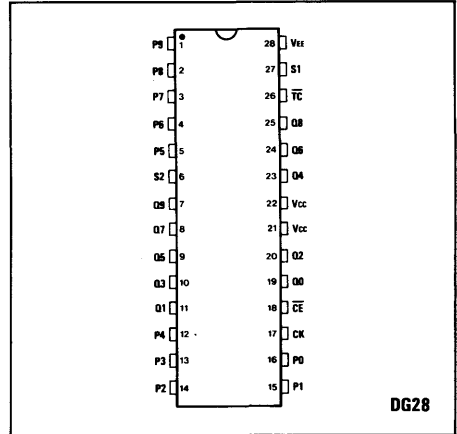


Fig.1 Pin connections - top view

### PIN NAMES

$P_n$	Preset Data Inputs
$Q_n$	Outputs
S1	Control Input
S2	Control Input
CK	Clock Input
$\overline{CE}$	Count Enable
$\overline{TC}$	Terminal Count
$V_{CC}$	Positive Supply (Ground)
$V_{EE}$	Negative Supply

**ELECTRICAL CHARACTERISTICS**

Each circuit has been designed to meet the d.c. specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

Characteristic		Symbol		Pin under test		TEST VOLTAGE APPLIED TO PINS LISTED BELOW										TEST VOLTAGE (V)					
						-30°C		+25°C		+85°C		Unit		V <sub>in</sub> Max.		V <sub>in</sub> Min.		V <sub>OL</sub> Max.		V <sub>OL</sub> Min.	
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Max.
<b>POWER SUPPLY</b>																					
Drain current	I <sub>EE</sub>	-	-	-	-	195	-	-	-	mAdc	-	-	-	-	-	-	-	28	21,22		
Input current	I <sub>EEI</sub>	-	-	-	-	450	-	-	-	μAdc	Note 1	-	-	-	-	-	-	28	21,22		
Input leakage current	I <sub>INL</sub>	-	-	-	-	0.5	-	-	-	μAdc	Note 1	-	-	-	-	-	-	28	21,22		
Logic '1' output voltage	V <sub>OH</sub>	-1.060	-0.890	-	-	-0.810	-	-0.89	-	Vdc	Data inputs	-	-	-	-	-	-	28	21,22		
Logic '0' output voltage	V <sub>OL</sub>	-1.89	-1.675	-	-	-1.650	-	-1.825	-	Vdc	-	-	-	-	-	-	-	28	21,22		
Logic '1' threshold voltage	V <sub>OH1</sub>	-1.080	-	-	-	-0.98	-	-0.910	-	Vdc	Data inputs	-	-	-	-	-	-	28	21,22		
Logic '0' threshold voltage	V <sub>OL0</sub>	-	-1.655	-	-	-1.630	-	-1.585	-	Vdc	-	-	-	-	-	-	-	28	21,22		
<b>SWITCHING TIMES</b>																					
Propagation delay (50 ohm load)	t <sub>p</sub>	-	-	-	-	2	12	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Clock input	t <sub>c</sub>	-	-	-	-	2	8	-	-	ns	-	-	-	-	-	-	-	28	21,22		
	t <sub>et</sub>	-	-	-	-	2	10	-	-	ns	S2	-	-	-	-	-	-	28	21,22		
	t <sub>et'</sub>	-	-	-	-	2	10	-	-	ns	S2	-	-	-	-	-	-	28	21,22		
Count enable - terminal count	t <sub>ec</sub>	-	-	-	-	2	5	-	-	ns	S2	-	-	-	-	-	-	28	21,22		
Set-up time	t <sub>su0</sub>	-	-	-	-	2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Data inputs	t <sub>suD</sub>	-	-	-	-	2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Select inputs	t <sub>suS</sub>	-	-	-	-	5.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
	t <sub>suS</sub>	-	-	-	-	5.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Count enable input	t <sub>suC</sub>	-	-	-	-	5.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
	t <sub>suC</sub>	-	-	-	-	5.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Hold time	t <sub>HO</sub>	-	-	-	-	-2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Data inputs	t <sub>HO</sub>	-	-	-	-	-2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Select inputs	t <sub>HO</sub>	-	-	-	-	-2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
	t <sub>HO</sub>	-	-	-	-	-2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Count enable input	t <sub>HO</sub>	-	-	-	-	-2.0	-	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Maximum counting frequency	f <sub>count</sub>	-	-	-	-	50	-	-	-	MHz	-	-	-	-	-	-	-	28	21,22		
Rise time 20 % - 80 %	t <sub>r</sub>	-	-	-	-	1.5	3.5	-	-	ns	-	-	-	-	-	-	-	28	21,22		
Fall time 20 % - 80 %	t <sub>f</sub>	-	-	-	-	1.5	3.0	-	-	ns	-	-	-	-	-	-	-	28	21,22		

NOTES  
 1. Each input pin tested individually.  
 2. Output level to be measured after a clock pulse has been applied.

TEST CIRCUIT DETAILS

NOTE

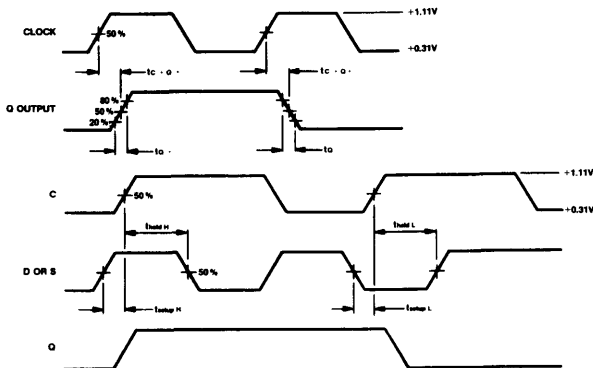
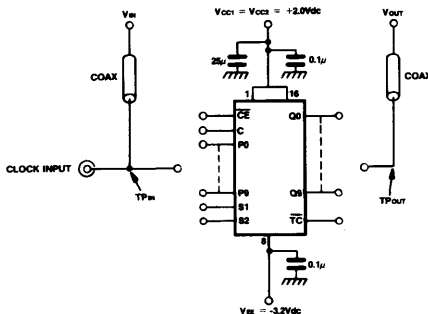
$t_{setup}$  is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

$t_{hold}$  is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse

$$t_+ = t_- = 2.0 \pm 0.2ns$$

(20 to 80 %)

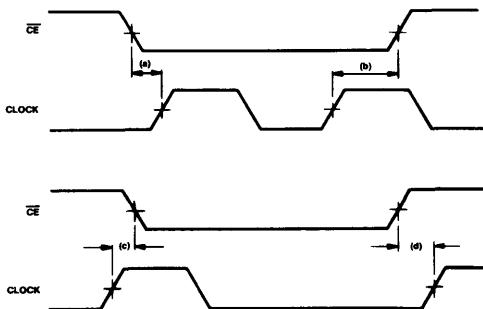


50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be  $\leq 1/4$  inch from TPIN to input pin and TPOUT to output pin.

Unused outputs are connected to a 50 ohm resistor to ground.

Fig.2 Switching time test circuit and waveforms at 25° C



(a) is the minimum time to wait after the counter has been enabled to clock it

(b) is the minimum time before the counter has been disabled that it may be clocked

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter

(b) and (c) may be negative numbers

Fig.3 Set up and hold times



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# SP9218

## 8 BIT ECL LATCHED ADDER

Voltage levels are ECL compatible. Input pull-down resistors eliminate the need to tie unused inputs to VEE.

### FEATURES

- 25nsec Maximum Add Time
- Input and Output Latches
- 25MHz System Operation (100MHz in Multiplex Mode)
- B Latch can be Externally Reset
- Latches can be Clocked Individually
- -30°C to +85°C Operation
- 5.2V Supply

### APPLICATIONS

- Pipelined Systems
- Digital Noise Reduction
- Video Picture Enhancement
- Adder/Subtractor or Accumulator

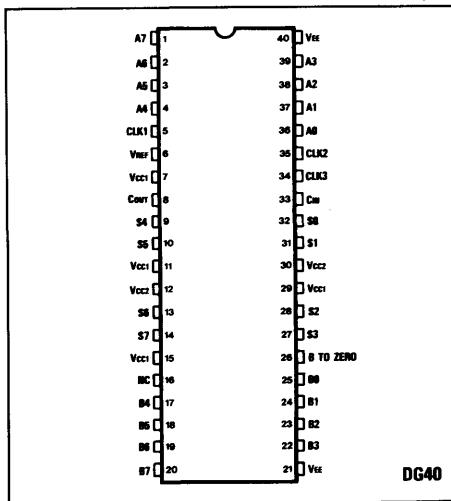


Fig.1 Pin connections - top view

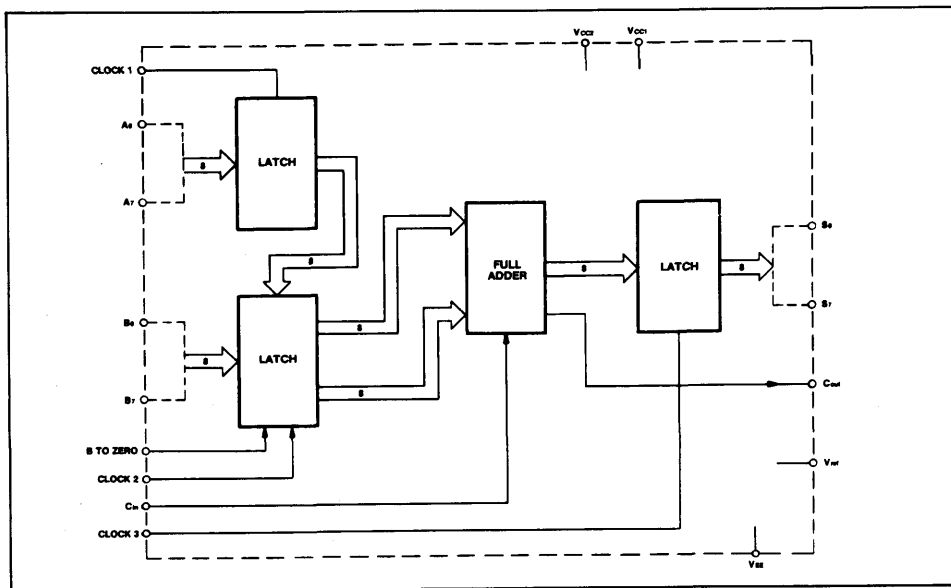
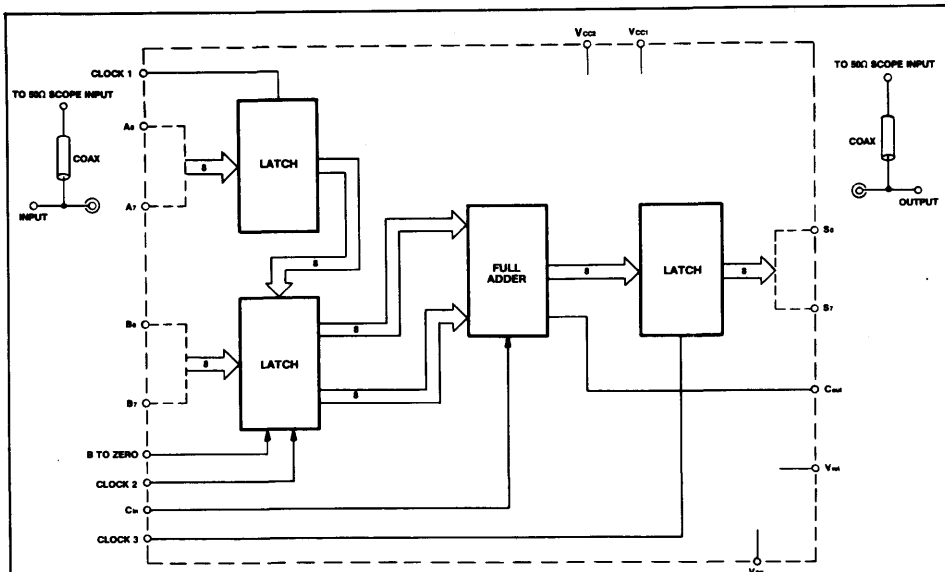


Fig.2 Internal block diagram





Supply voltages at 2V and -3.2V enable outputs to be terminated by 50 ohm to ground. All input and output cables to the scope are equal lengths of 50 ohm coaxial cable terminated by 50 ohm located in each scope channel input. The B to Zero is normally low, high will clear B latch.

Fig.3 Test circuit details

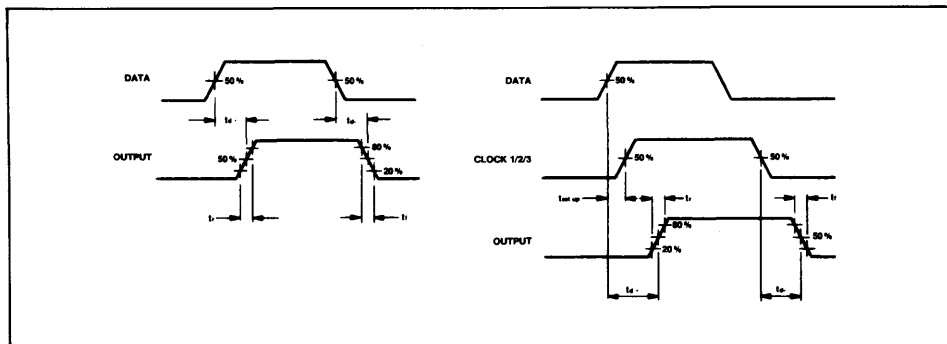


Fig.4 Timing waveforms





# SP9680

## ULTRA FAST COMPARATOR

The SP9680 is an ultra fast comparator manufactured using a high performance bipolar process which makes possible very short propagation delays (2.4ns typ.).

The circuit has differential inputs and complementary ECL outputs, capable of driving 50 Ω lines.

The device is manufactured in a low cost mini-dip package and is intended as an alternative to the faster SP9685 in applications where performance premium and the latch facility are not required.

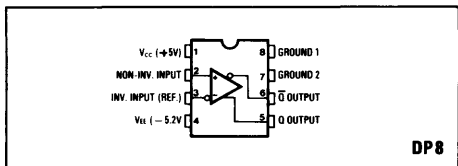


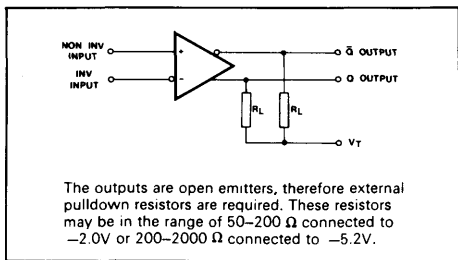
Fig. 1 Pin connections

### FEATURES

- Propagation Delay 2.4ns Typ.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- 8-Lead Plastic Package

### QUICK REFERENCE DATA

- Supply Voltages +5, -5.2V
- Operating Temperature Range -30°C to +70°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to -2.0V or 200–2000 Ω connected to -5.2V.

Fig. 2 Functional diagram

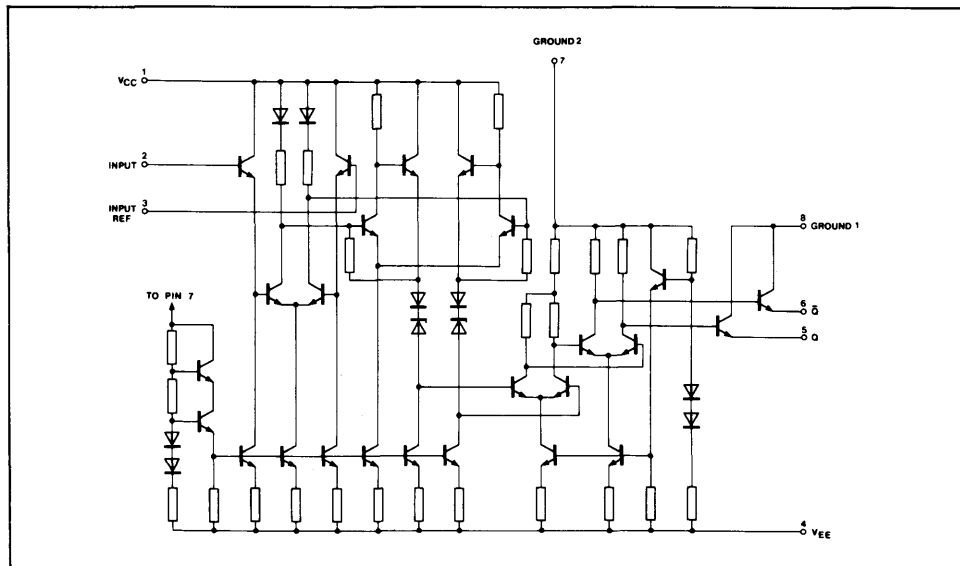


Fig. 3 SP9680 circuit diagram

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated):

- $T_{amb} = 25^{\circ}C$
- $V_{CC} = 5.00V \pm 0.25V$
- $V_{EE} = -5.2V \pm 0.25V$
- $R_L = 50 \Omega$
- $V_T = -2.0V$  (See Fig. 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	-6		+6	mV	} 100mV pulse, 10mV overdrive
Input bias current		20	40	$\mu A$	
Input offset current			10	$\mu A$	
Supply current $I_{CC}$		18	25	mA	
Supply current $I_{EE}$		22	35	mA	
Total power dissipation		200	300	mW	
Input to Q output delay		2.4	4	ns	
Input to $\bar{Q}$ output delay		2.4	4	ns	
Common mode range	-2		+2	V	
Common mode rejection ratio		80		dB	
Output logic levels					
Output HIGH	-0.96		-0.81	V	
Output LOW	-1.85		-1.65	V	
Input capacitance		3.5		pF	
Input resistance	50			$k\Omega$	
Operating temperature range	-30		+70	$^{\circ}C$	

**ABSOLUTE MAXIMUM RATINGS**

- Positive supply voltage  $V_{CC} +6V$
- Negative supply voltage  $V_{EE} -6V$
- Output current 30mA
- Input voltage  $\pm 3V$
- Differential input voltage 3.5V
- Storage temperature  $-55^{\circ}C$  to  $+125^{\circ}C$



# SP9685

## ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-and-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and -5.2V rails.

### FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- Supply +5V, -5.2V
- Operating Temperature Range -30°C to +85°C
- 50 Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM685 — But Faster

### ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	-6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Power dissipation	336mW
Storage	-55°C to +150°C
Lead temperature (soldering 60 sec)	300°C

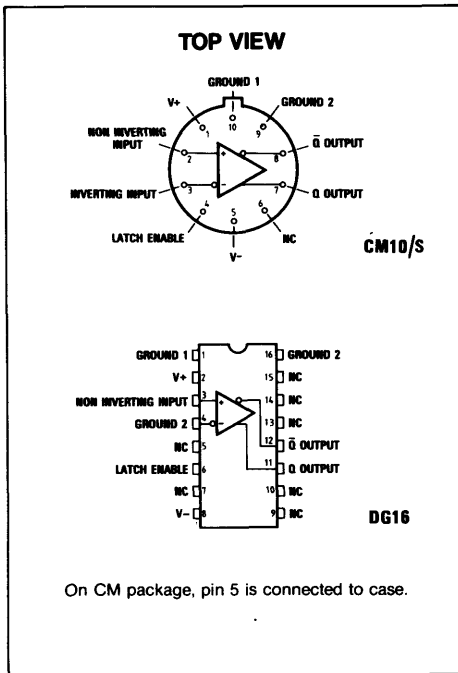


Fig. 1 Pin connections

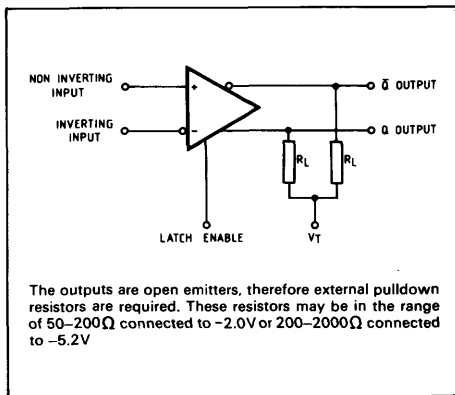


Fig. 2 Functional diagram

**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated) :

- $T_{AMB} = 25^{\circ}C$
- $V_{CC} = +5.0V \pm .25V$
- $V_{EE} = -5.2V \pm .25V$
- $R_L = 50\Omega; V_T = -2.0V$  (See Fig.2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	-5		+5	mV	Rs <100 $\Omega$
Input bias current		10	20	$\mu A$	
Input offset current			5	$\mu A$	
Supply currents I <sub>CC</sub>		19	23	mA	
I <sub>EE</sub>		23	34	mA	
Total power dissipation		210	330	mW	
Min. latch set-up time (t <sub>s</sub> )		0.5	1	ns	
Input to Q output delay (t <sub>pd</sub> )		2.2	3	ns	
Input to $\bar{Q}$ output delay (t <sub>pd</sub> )		2.2	3	ns	
Latch to Q delay t <sub>pd(E)</sub>		2.5	3	ns	
Latch to $\bar{Q}$ delay t <sub>pd(E)</sub>		2.5	3	ns	
Min. latch pulse width t <sub>pw(E)</sub>		2	3	ns	
Min. hold time (t <sub>h</sub> )			1	ns	
Common mode range	-2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			k $\Omega$	
Input & output logic levels					At nominal supply voltages, see Fig. 4
Output High	-.96		-.81	V	
Output Low	-1.85		-1.65	V	
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

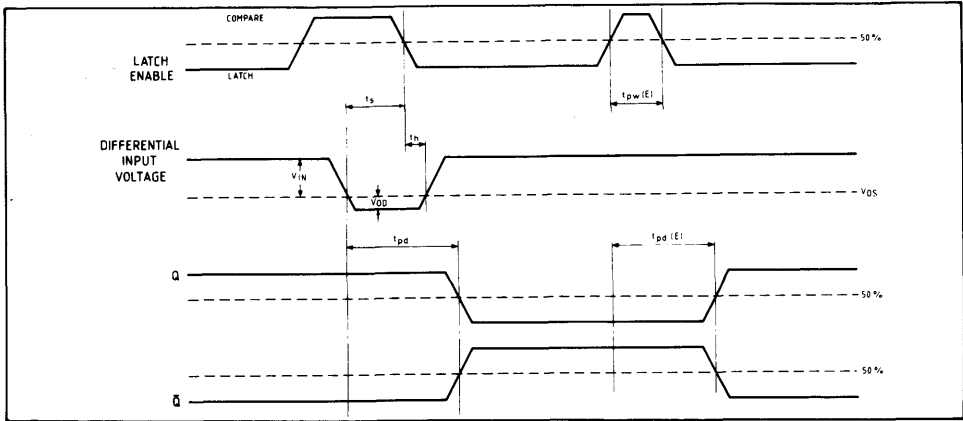


Fig.3 Timing diagram

**OPERATING NOTES**

**Timing diagram**

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time t<sub>pd</sub>. Output Q and  $\bar{Q}$

transitions are essentially similar in timing. The input signal must occur at a time t<sub>s</sub> before the latch falling edge, and must be maintained for a time t<sub>h</sub> after the latch falling edge, in order to be acquired. After t<sub>h</sub>, the output ignores the input status until the latch is again strobed. A minimum latch pulse width t<sub>pw(E)</sub> is required for the strobe operation, and the output transitions occur after a time t<sub>pd(E)</sub>.

**Measurement of propagation and latch delays**

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.



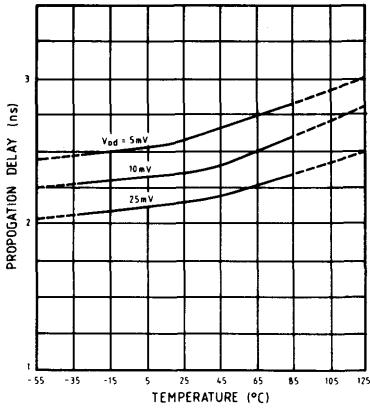


Fig.10 Propagation delay, input to output as a function of temperature

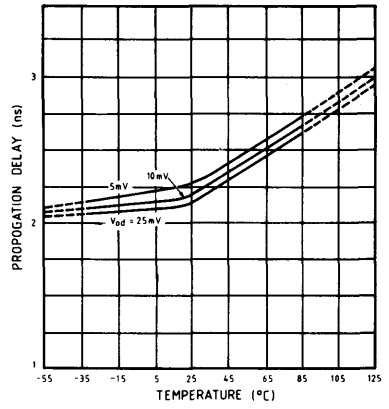


Fig.11 Propagation delay, latch to output as a function of temperature

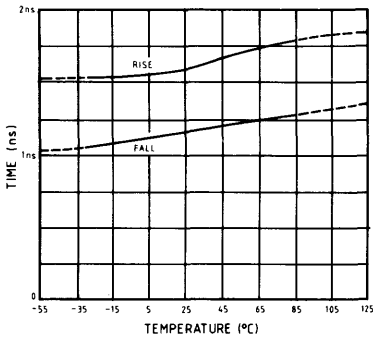


Fig.12 Output rise and fall times as a function of temperature

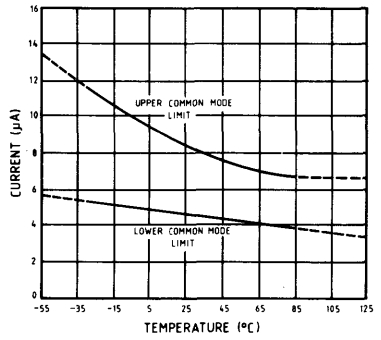


Fig.13 Input bias currents as a function of temperature

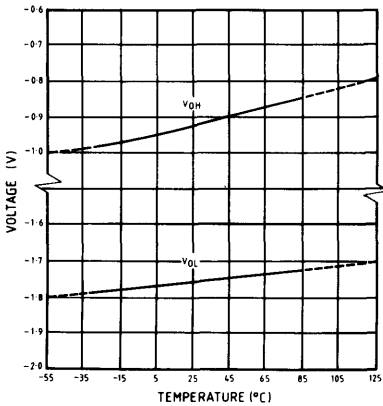


Fig.14 Output levels as a function of temperature

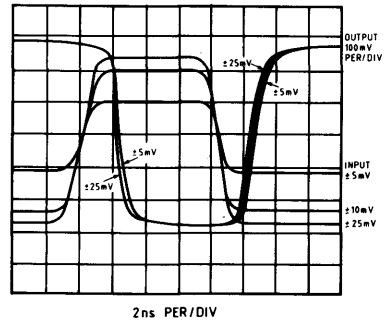


Fig.15 Response to various input signal levels

# SP9687

## ULTRA FAST DUAL COMPARATOR

The SP9687 is an ultra-fast, dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and  $\bar{L}E$  is low, the comparator function is in operation. When LE is driven low and  $\bar{L}E$  high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, LE must be connected to ground.

The device is pin compatible with the AM687 and operates from conventional +5V and -5.2V rails.

### FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- 50Ω Line Driving Capability
- Excellent Common Mode Rejection
- Supply Voltages +5V, -5.2V
- Operating Temperature Range -30°C to +85°C
- Pin Compatible with AM687 — But Faster
- Comparators within each SP9687 are matched as follows:  
Input to Output Delay 200ps (typ)  
Latch to Output Delay 200ps (typ)

### OPERATING NOTES

#### Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse, switches the comparator over after a time  $t_{pd}$ . Output Q and  $\bar{Q}$  transitions are essentially similar in timing. The input signal must occur at a time  $t_s$  before the latch falling edge, and must be maintained for a time  $t_h$  after the

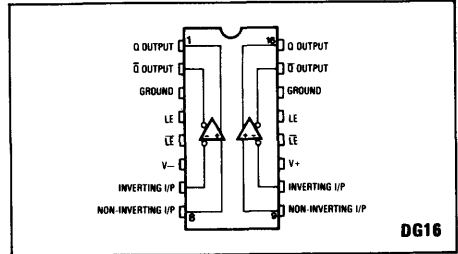
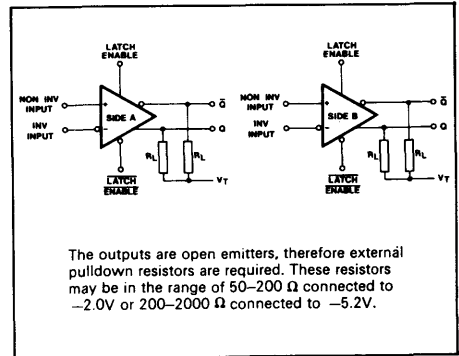


Fig. 1 Pin connections



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to -2.0V or 200–2000 Ω connected to -5.2V.

Fig. 2 Functional diagram

### ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	-6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Differential latch voltage	3.5V
Power dissipation	590mW
Storage	-55° C to +125° C
Lead temperature (soldering 60 sec)	300° C

latch falling edge, in order to be acquired. After  $t_h$ , the output ignores the input status until the latch is again strobed. A minimum latch pulse with  $t_{pw(E)}$  is required for the strobe operation, and the output transitions occur after a time  $t_{pd(E)}$ . The  $\bar{L}E$  input is omitted for clarity.



**ELECTRICAL CHARACTERISTICS**

Test conditions (unless otherwise stated) :

- $T_{AMB} = 25^{\circ}C$
- $V_{CC} = +5.00V \pm .25V$
- $V_{EE} = -5.20V \pm .25V$
- $R_L = 50\Omega$
- $V_T = -2.0V$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	-5		+5	mV	Rs <100Ω
Input bias current		5	20	μA	
Input offset current		1	5	μA	} Note 3
Supply currents I <sub>CC</sub>		30	46	mA	
I <sub>EE</sub>		54	68	mA	} Nominal conditions
Total power dissipation		430	590	mW	
Min. latch set-up time (t <sub>s</sub> )		0.5	1	ns	} Notes 1,2
Input to Q output delay (t <sub>pd</sub> )		2.2	3	ns	
Input to Q̄ output delay (t <sub>pd</sub> )		2.2	3	ns	} 100 mV pulse } note 1
Latch to Q delay t <sub>pd</sub> (E)		2.5	3	ns	
Latch to Q̄ delay t <sub>pd</sub> (E)		2.5	3	ns	} Notes 1,2
Min. latch pulse width t <sub>pw</sub> (E)		2	3	ns	
Min. hold time (t <sub>h</sub> )			1	ns	
Common mode range	-2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			kΩ	
Input & output logic levels					
Output High	- .96		- .81	V	At nominal supply voltages
Output Low	-1.85		-1.65	V	
Operating temperature range	-30°		+85°	°C	
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

NOTES

1. These measurements are defined under conditions of a +100mV pulse with -10mV overdrive. The relationship between overdrive and delay is illustrated in Figs. 6 to 8.
2. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.
3. Refers to the entire package. Other data in this table applies to each half device.

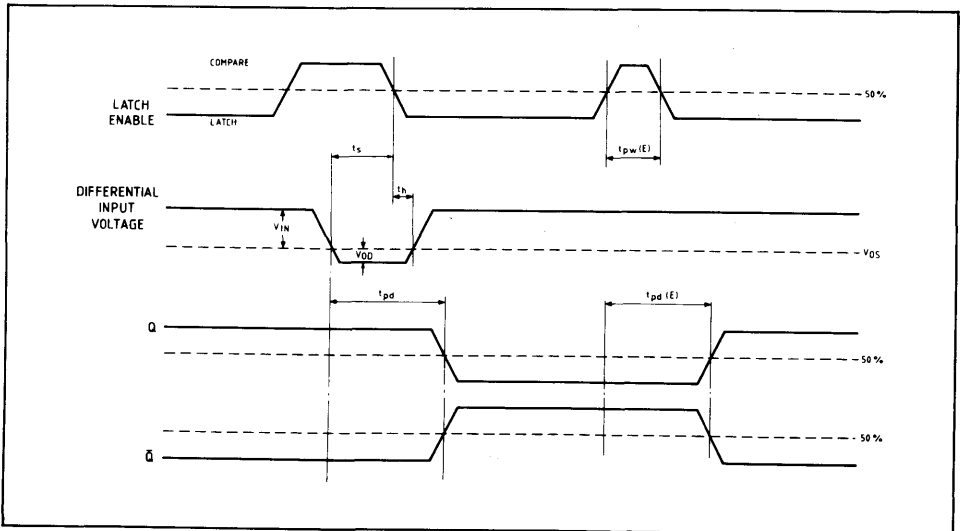


Fig. 3 Timing diagram

**PERFORMANCE CURVES**

Unless otherwise specified, standard conditions for all curves are  $T_{AMB} = 25^{\circ}C$ ,  $V_{CC} = 5.0V$ ,  $V_{EE} = -5.2V$

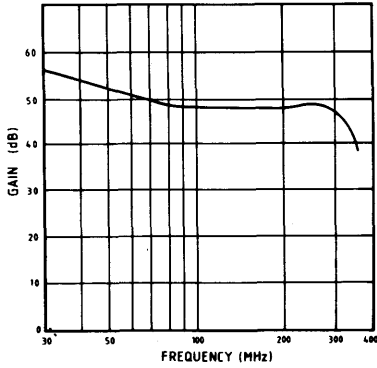


Fig. 4 Open loop gain as a function of frequency

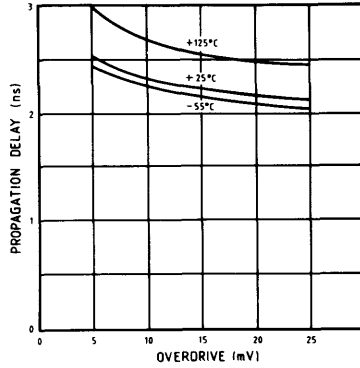


Fig. 5 Propagation delay, latch to output as a function of overdrive

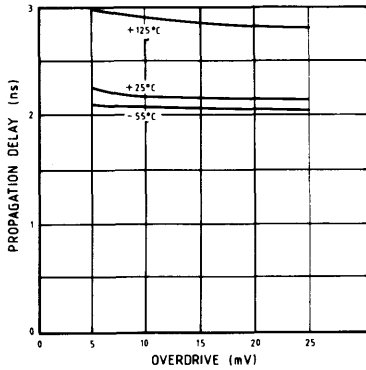


Fig. 6 Propagation delay, input to output as a function of overdrive

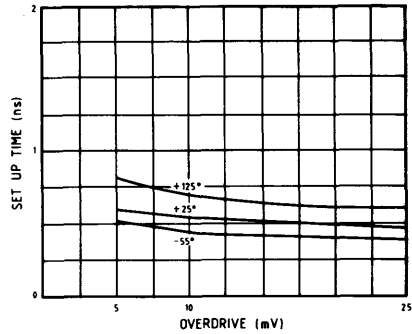


Fig. 7 Set-up time as a function of input overdrive

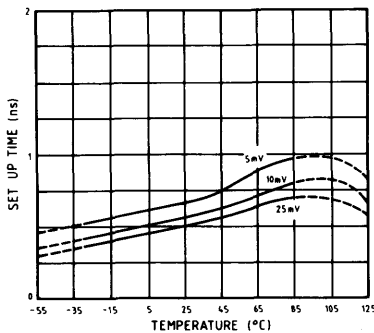


Fig. 8 Set-up time as a function of temperature

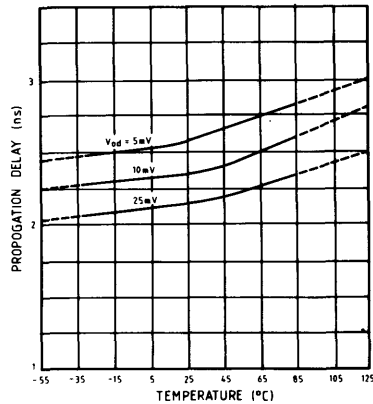


Fig. 9 Propagation delay, input to output as a function of temperature

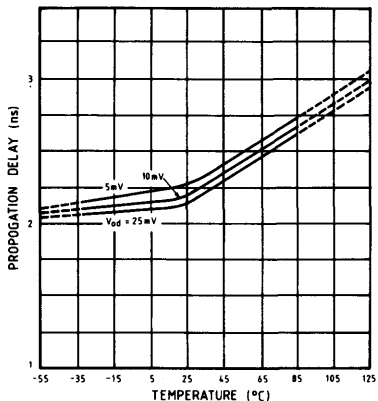


Fig. 10 Propagation delay, latch to output as a function of temperature

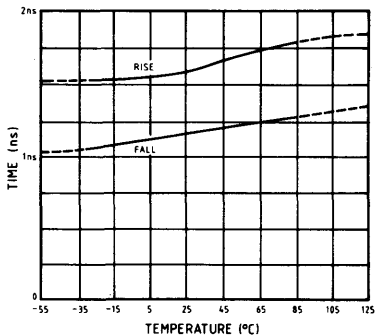


Fig. 11 Output rise and fall times as a function of temperature

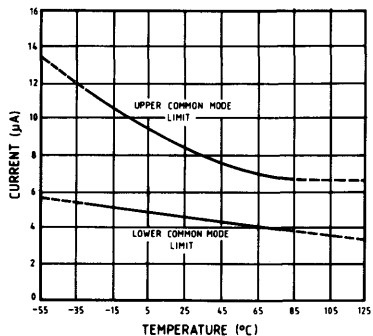


Fig. 12 Input bias currents as a function of temperature

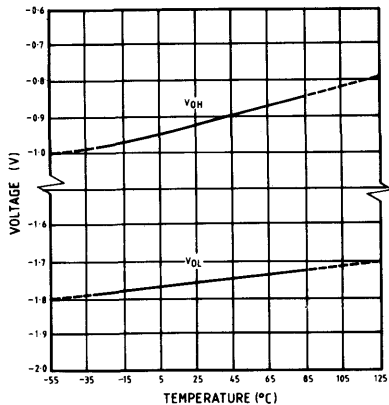


Fig. 13 Output levels as a function of temperature

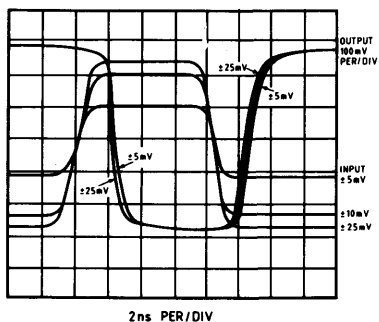


Fig. 14 Response to various input signal levels.

# SP9754

## FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A-D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110MHz, with analogue inputs up to Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous and valid for the complete clock period.

The SP9754 operates from a +5V, -7V supply.

### FEATURES

- No External Components For 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding For Expansion to 8 Bits
- No External Sample and Hold Needed
- On-Chip Resistor Reference Divider
- Bit Size 10-100mV
- ECL Compatible
- Over 50MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy

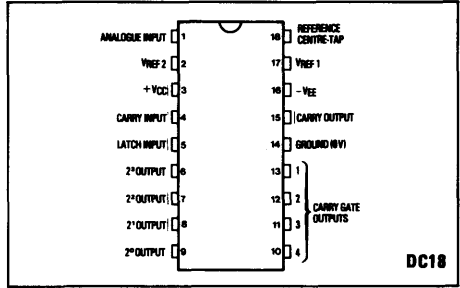


Fig.1 Pin connections

### ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Operating temperature range	-30° C to +85° C
Storage temperature	-55° C to +125° C
Lead temperature (soldering 60s)	300° C

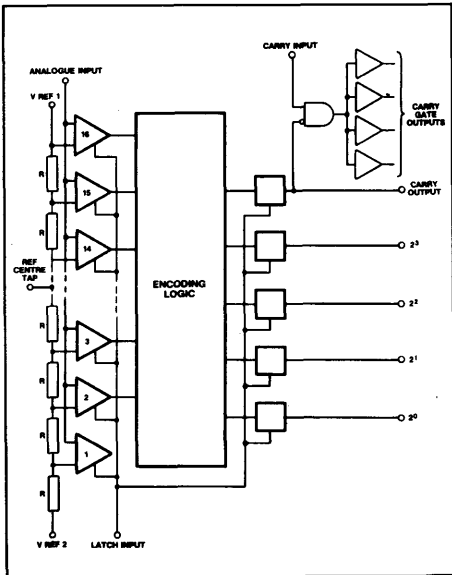


Fig.2 Functional diagram

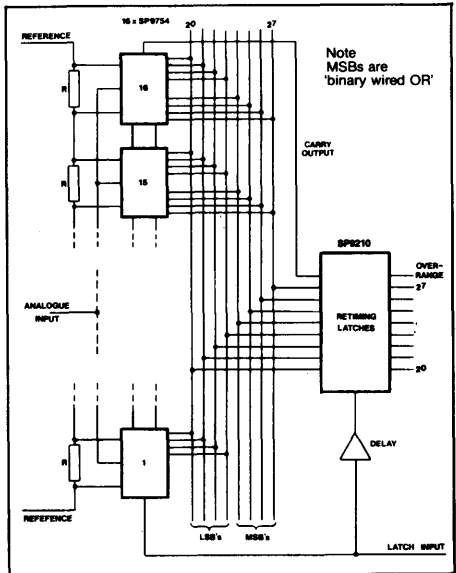


Fig.3 8-bit all-parallel system

**ELECTRICAL CHARACTERISTICS**

**Test conditions (unless otherwise stated):**

- $T_{AMB} = 25^{\circ}C$
- $V_{CC} = +5V \pm 0.25V$
- $V_{EE} = -7V \pm 0.25V$
- $R_L = 100\text{ohms to } -2V$

Characteristic	Symbol	Value			Units	Conditions	
		Min.	Typ.	Max.			
Analogue input current	$I_B$		30	100	$\mu A$	$V_{IN} = 0V$	
Analogue input capacitance	$C_{IN}$		10		pF		
Common mode range	$V_{CM}$	-2		+2	V	} See Fig.11 total	
Maximum input slew rate			1000		V/ $\mu$ sec		
Latch input capacitance	$C_{IN}$		2		pF		
Positive supply current	$I_{CC}$		55	70	mA		
Negative supply current	$I_{EE}$		85	100	mA		
Reference resistor chain			25		$\Omega$		
Reference bit size		10		100	mV		
Comparator offset voltage	$V_{OS}$	-5		+5	mV		
Total power dissipation	$P_{DISS}$		950	1160	mW		All outputs loaded
Input & output logic levels							for 100 ohm load to -2V
Logic high	$V_{OH}$	-0.930		-0.720	V		
Logic low	$V_{OL}$	-1.90		-1.620	V		
Min. latch set-up time	$t_s$		1.5	2	nsec	10mV overdrive	
Latch to output propagation delay:							
Latch enable to output high	$t_{pd} + (E)$		6	8	nsec		
Latch enable to output low	$t_{pd} - (E)$		5	8	nsec		
Carry input to MSB delay	$t_{pd} (C)$		3	5	nsec		
Max. sample rate	$F_c \text{ max.}$	100	110		MHz		
Aperture uncertainty time	$t_a$		10		psec		

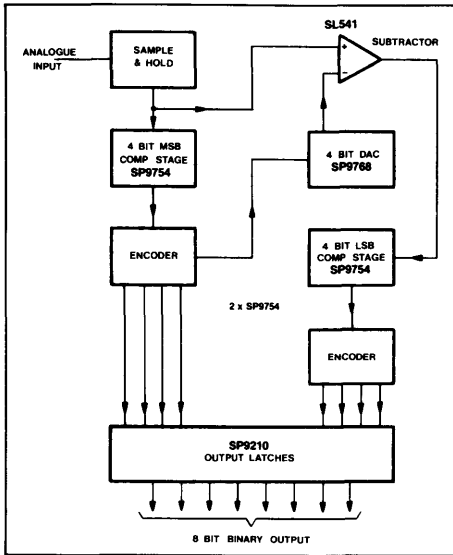


Fig.4 Parallel-series-parallel system

**PERFORMANCE CURVES**

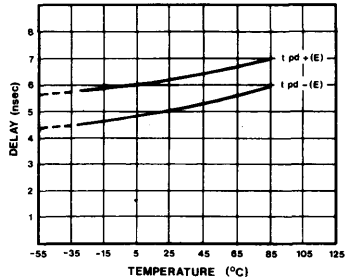


Fig.5 Latch to output propagation delay as a function of temperature

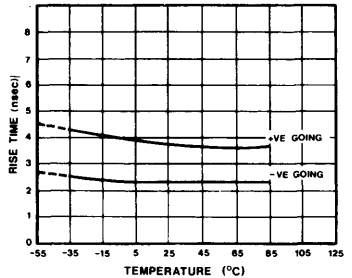


Fig.6 Output risefall times as a function of temperature

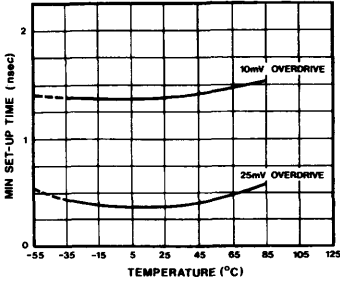


Fig.7 Set-up time as a function of temperature

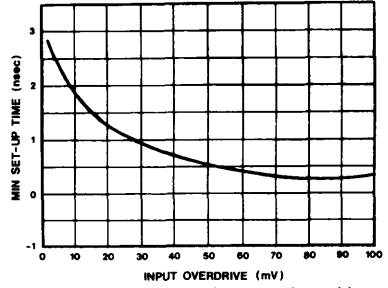


Fig.8 Set-up time as a function of overdrive

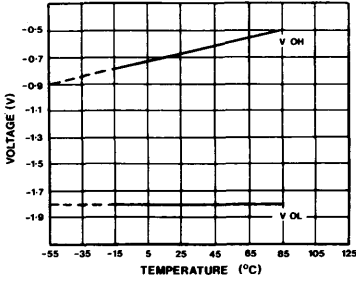


Fig.9 Output logic levels as a function of temperature

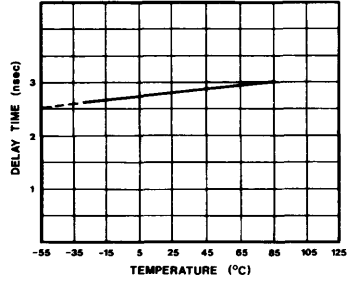


Fig.10 Carry input to MSB output delay as a function of temperature

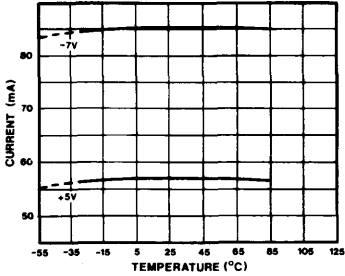


Fig.11 Supply current as a function of temperature

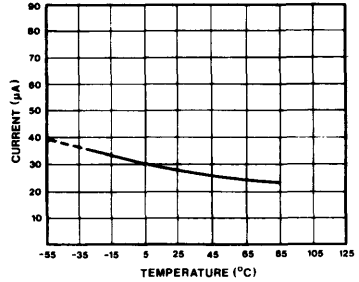


Fig.12 Analogue input current as a function of temperature

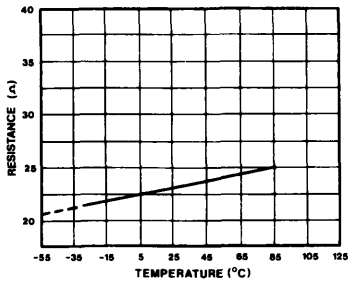


Fig.13 Network resistance as a function of temperature

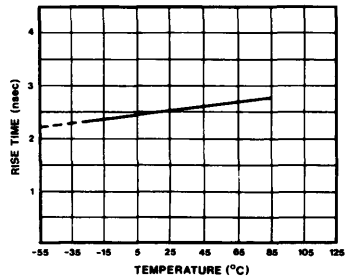


Fig.14 MSB output edge speeds as a function of temperature

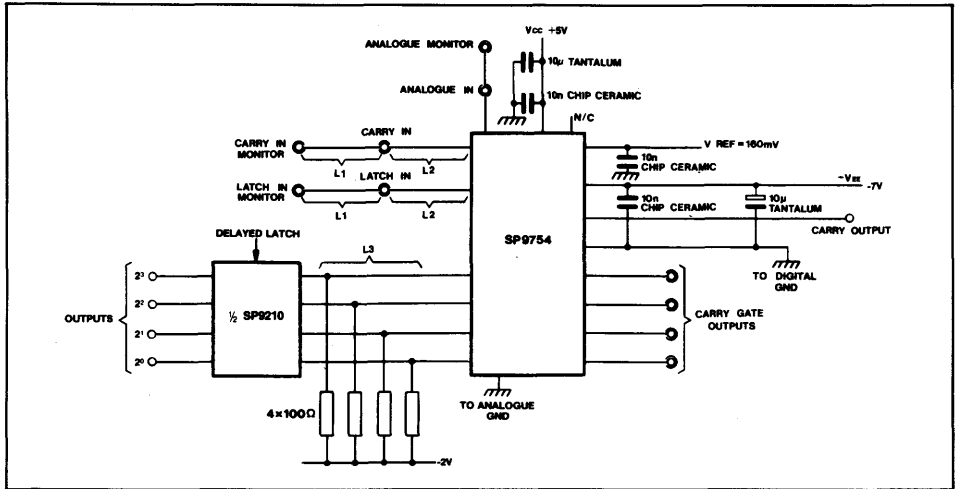


Fig.15 High frequency test circuit  
 NOTE At latch frequencies below 60MHz the SP9210 can be omitted.

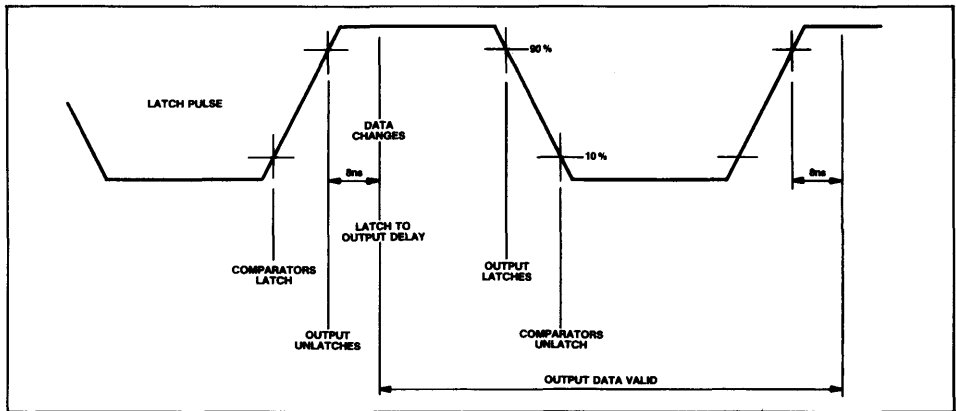


Fig.16 Timing diagram

**OPERATING NOTES**

1. Carry output (pin 15) is high when the analogue input exceeds the top reference voltage (pin 17).  
 Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4). When the analogue input is between  $V_{REF}$  and  $V_{REF2}$  and the carry output is low, the carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.
2. When used in an ambient temperature in excess of 45° C the SP9754 must be provided with an external electrically isolated heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 150° C (thermal resistance junction/case 35° C per watt).

# SP9768

## 8 BIT DIGITAL TO ANALOGUE CONVERTER

The SP9768 is capable of converting an 8-bit digital signal into an analogue voltage at a rate of over 100 mega-samples per second. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. Included on the chip are a precision voltage reference and a reference amplifier.

### FEATURES

- 5ns Setting Time to 1/2 LSB
- ECL Inputs, Current Output
- Voltage Reference Temp. Coeff. 50 ppm/°C
- Over 100 MBits/S Update Rate
- 40MHz Multiplying Mode
- Operating Temperature Range -30°C to +85°C

### APPLICATIONS

- Data Conversion
- Instrumentation
- Video Speed Successive Approximation ADCs
- Video Graphic Displays

### QUICK REFERENCE DATA

Supply voltages: +5V, -5.2V  
Power consumption: 400mW

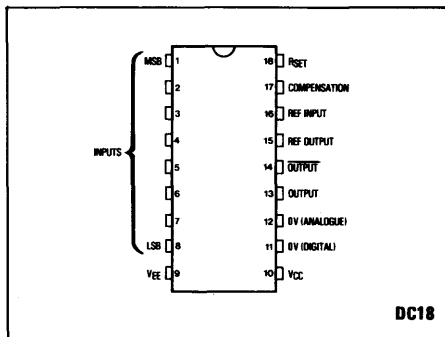


Fig.1 Pin connections

### ABSOLUTE MAXIMUM RATINGS

Supply voltage: -6V, +6V  
Storage temperature: -55°C to +125°C  
Operating temperature range: -30°C to +85°C

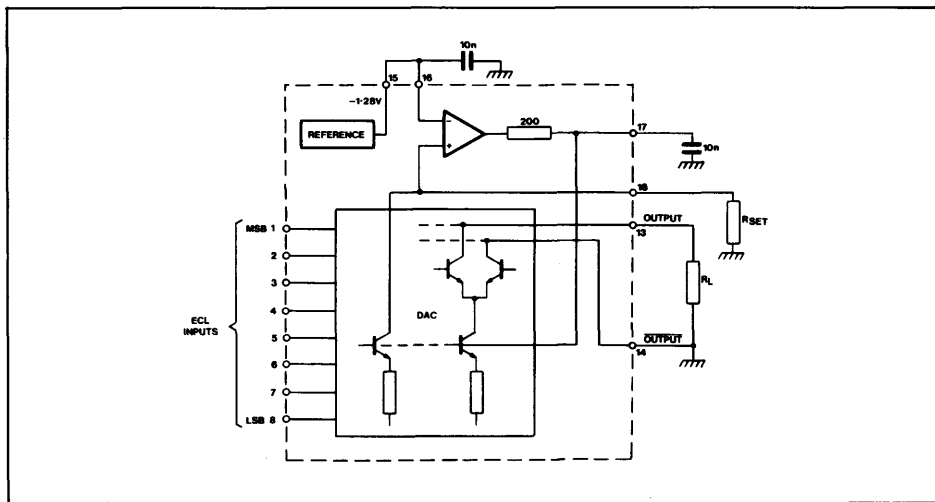


Fig.2 SP9768 block diagram



ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

- T<sub>amb</sub> 25°C
- V<sub>CC</sub> +5.00V ± 5%
- V<sub>EE</sub> -5.20V ± 5%
- R<sub>L</sub> = 50Ω
- R<sub>set</sub> = 220Ω
- Input voltage High -0.96V (min) -0.81V (max)
- Low -1.85V (min) -1.65V (max)

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Differential non-linearity			0.2	%	
Absolute non-linearity			0.2	%	
Settling time		5		ns	See Operating Note 1
Nominal bit size		78		μA	R <sub>L</sub> = 50Ω } R <sub>set</sub> = 220Ω
		4		mV	
Positive output compliance		+3		V	
Negative output compliance	-1			V	25°C } see Operating Note 2
	-0.7			V	
Multiplying bandwidth		40		MHz	Current mode, see Operating Note 3
Maximum full scale output			30	mA	
Minimum full scale output	2			mA	
Reference voltage		-1.28		V	
Temp coeff of reference voltage		20		ppm/°C	
Zero output		60		μA	
Output current symmetry		100		μA	
Supply current (I <sub>CC</sub> )		12	20	mA	
(I <sub>EE</sub> )		66	80	mA	

CIRCUIT DESCRIPTION

The DAC has current outputs, with a nominal full scale of 20mA, corresponding to a 1volt drop across a 50ohm load, or ±1volt across 100ohms returned to +1 volt. See Operating Note 2.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I<sub>OUT</sub>, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I<sub>OUT</sub> is also provided. The setting resistor, R<sub>SET</sub>, is typically 220ohms, and should have a temperature coefficient similar to that of the output load resistor.

Where the load is an oscilloscope, with a 50ohm

nominal input, a good quality metal oxide resistor should be used for R<sub>SET</sub>. It is important to realise that reflections present in 50ohm load systems will often prove to be a limiting factor in the measurement of settling time.

The reference voltage source is nominally 1.280volts and is of a modified bandgap type, average temperature coefficient of 20ppm/°C over the range -55°C to +125°C, corresponding to approximately 1LSB change over this temperature range.

To reduce the possibility of instability or noise generation, the reference supply (pin 15) can be decoupled using a high quality ceramic chip capacitor. Stabilisation of the loop amplifier is by a single capacitor from pin 17 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

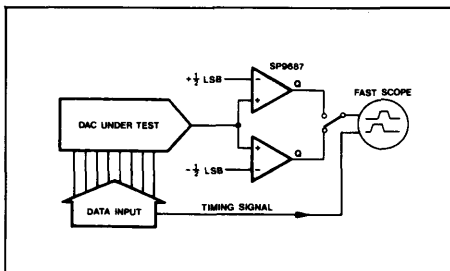


Fig.3 Test schematic (settling time)

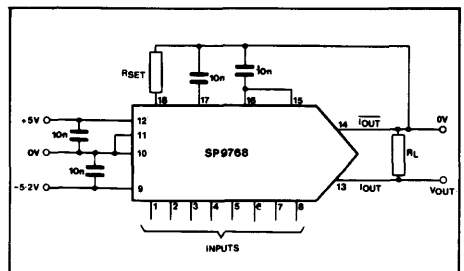


Fig.4 Conventional DAC. Negative output wrt ground.

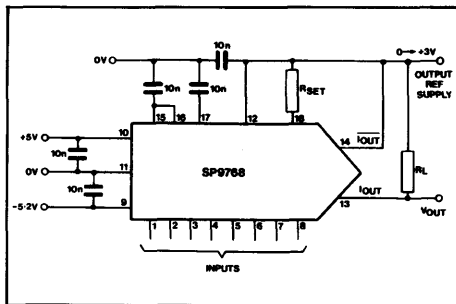


Fig.5 Voltage output referred to positive supply

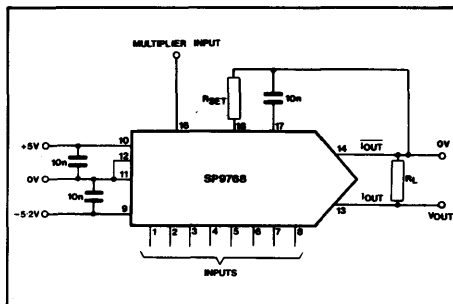


Fig.6 Multiplying DAC (Voltage mode)

**OPERATING NOTES**

**1. Measurement of Settling Time**

The settling time of the SP9768 is measured for a worst case transition of 0 to full scale.

Oscilloscopes, whether real time or sampling, do not have sufficiently low input VSWR or on-screen resolution for precise settling time measurements. A measurement technique has been designed, shown diagrammatically in Fig.3, in which the DAC can settle into a nearly ideal 50ohm load, with minimal interconnection paths; this is also very closely related to the practical use of the device. Precision settling time measurements can be performed with a high speed comparator, conveniently a dual device, such as the SP9687, with a minimal delay time, in this case about 2ns. Two references are set up to detect the DAC output settling within a window, conveniently defined as the settling to ground of the output.

The lower comparator detects the DAC output coming within 1/2 LSB of the final settling point, while the upper device checks that there is less than 1/2 LSB of over shoot.

**2. Output Compliance**

Fig.5 shows the method of using the SP9768 with a load resistor not referred to ground. This connection will be used most often when a larger output voltage than that permitted by the -0.7volt negative output voltage compliance specification is required. The output resistor can be referred to a positive supply in this case as long as R<sub>set</sub> and the analogue ground are also referred to this voltage. If I<sub>OUT</sub>

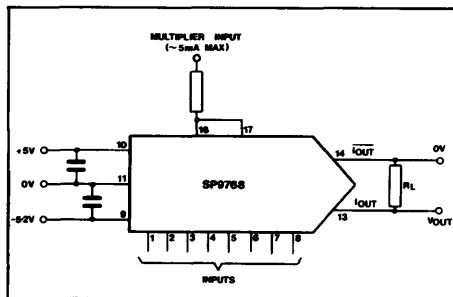


Fig.7 Multiplying DAC (Current mode)

is also connected to this reference the decoupling will be simplified.

**3. Multiplication Modes**

Multiplying operation of the DAC is available in two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3dB bandwidth is 250kHz, while in the latter, operational use exceeds 40MHz. Suggested circuits are shown in Figs. 6 and 7.

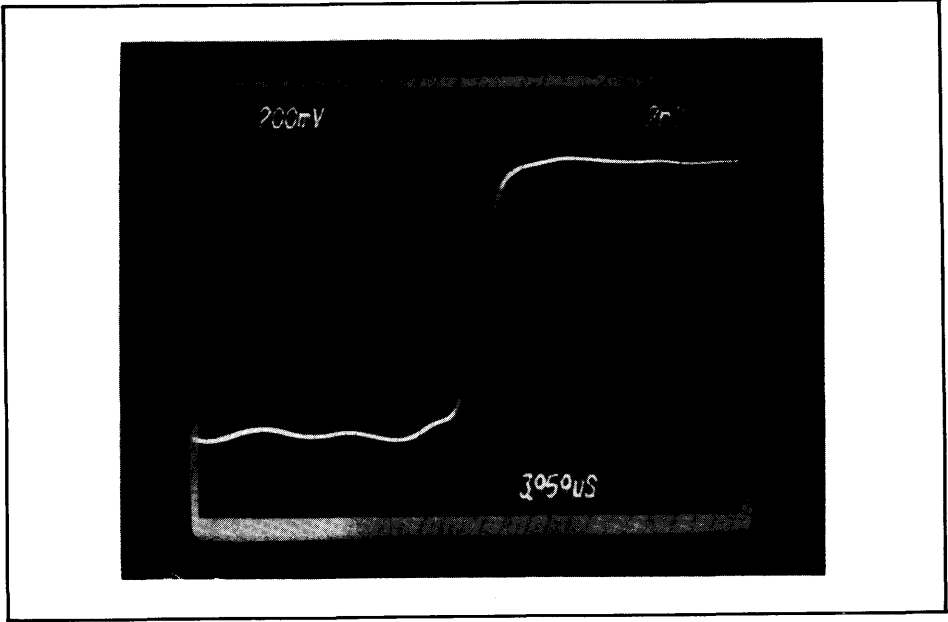


Fig.8 Full scale transition of Iout into 50 ohm using 1GHz bandwidth oscilloscope

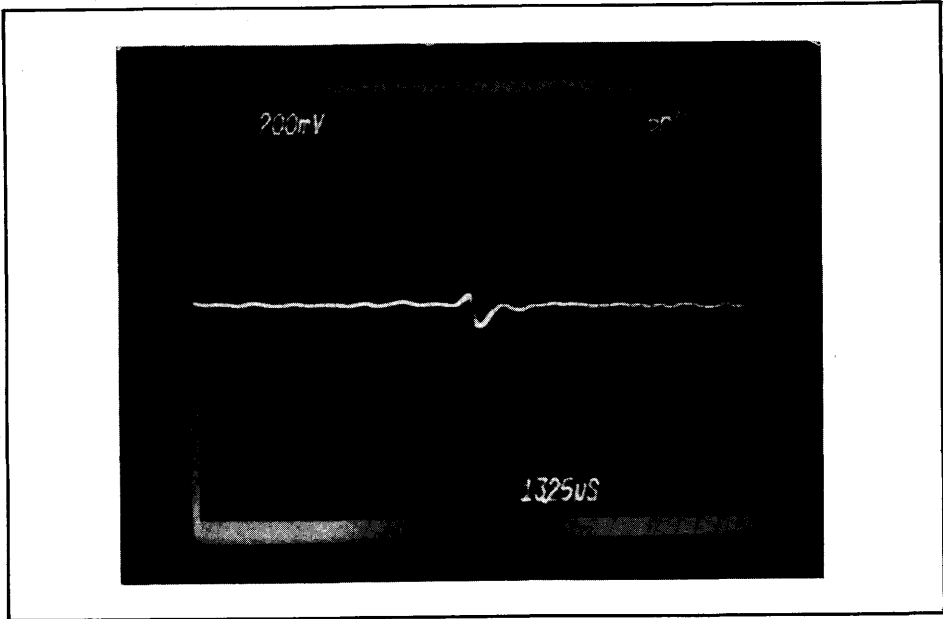


Fig.9 Typical centre point low energy glitch using 1GHz bandwidth oscilloscope



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# SP9770B

## 10-BIT HIGH SPEED MULTIPLYING D-A CONVERTER

The SP9770B is an ECL 10k compatible 10-bit DAC. The 12nsec settling time allows a 75 megasample per second conversion time. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP9770B design includes a high performance voltage reference and reference amplifier.

### FEATURES

- 12ns Settling Time
- 10 Bits to  $\pm 1/2$  LSB Absolute and Differential Non-linearity
- 75 MSPS Update Rate
- Current Output
- ECL 10K Standard Inputs
- Complementary Outputs, 20mA Full Scale
- Reference Temperature Coefficient Typically 40ppm/ $^{\circ}$ C
- Multiplying Mode Up To 20MHz

### APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems

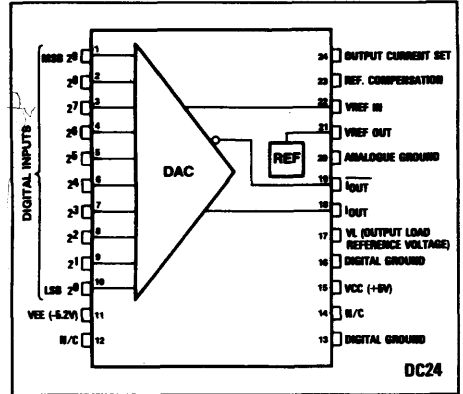


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-5.7V
Digital input voltage	0 to VEE
Maximum output load	2k $\Omega$
Output reference supply	0 to 3V
Operating temperature range	-30 $^{\circ}$ C to 85 $^{\circ}$ C
Storage temperature	-55 $^{\circ}$ C to 125 $^{\circ}$ C
Lead temperature (soldering 60 sec)	300 $^{\circ}$ C
Min.current set resistance RSET MIN.	150 $\Omega$

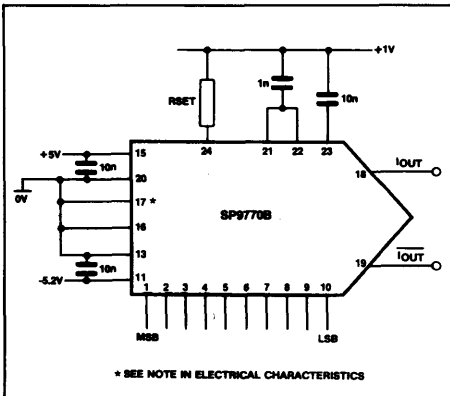


Fig.2(a) Conventional D/A operation using on-chip reference

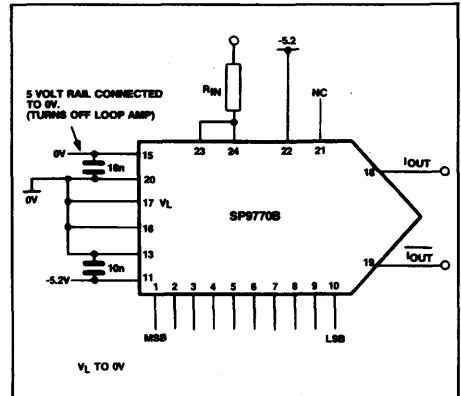


Fig.2(b) Multiplying mode operation (current mode)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = 25^{\circ}C$ ;  $V_{CC} = +5.00V \pm 5\%$ ;  $V_{EE} = -5.2V \pm 5\%$ ;  $R_{SET} = 240\Omega$ ; Input voltage: High = -0.810, Low = -1.850

Characteristic	Value			Units	Comments
	Min.	Typ.	Max.		
Reference voltage	-1.250	-1.280	-1.300	V	$I_{OUT} = V_{REF} \times 4 / R_{SET}$
Reference voltage temp. coefficient		40	80	ppm/ $^{\circ}C$	
Output current - full scale	2	20	30	mA	
Inputs					} Standard ECL 10k compatible All inputs high Current output Into 50 $\Omega$ load To 1 LSB Current mode
Voltage high	-0.96		-0.81	V	
Voltage low	-1.85		-1.65	V	
Current $I_{INH}$		115	200	$\mu A$	
Bit size $R_{SET} = 240$	19	21	23	$\mu A$	
Bit size $R_{SET} = 240$	0.9	1	1.1	mV	
Setting time - full scale		12	20	ns	
Multiplying bandwidth 3dB		25		MHz	
Resolution	10		10	Bits	
Differential non-linearity			0.098	%	
Absolute non-linearity			0.05	%	
Output compliance	-0.7		+1	V	At 85 $^{\circ}C$ See note At 25 $^{\circ}C$
	-1		+1	V	
Supply voltage $V_{CC}$	+4.75	+5	+5.25	V dc	
Supply voltage $V_{EE}$	-4.85	-5.2	-5.45	V dc	
Supply current $I_{CC}$	7	12	17	mA dc	
Supply current $I_{EE}$	45	56	70	mA dc	

NOTE

Output compliance (refer to Fig.4)

Pin 17 should be connected to a reference voltage supply at the most positive voltages required, with the load and  $R_{SET}$  pin 24 returned similarly to this reference. Conveniently, the reference is ground, but this limits the output to negative voltage excursions only. The output compliance can be increased at the expense of linearity.

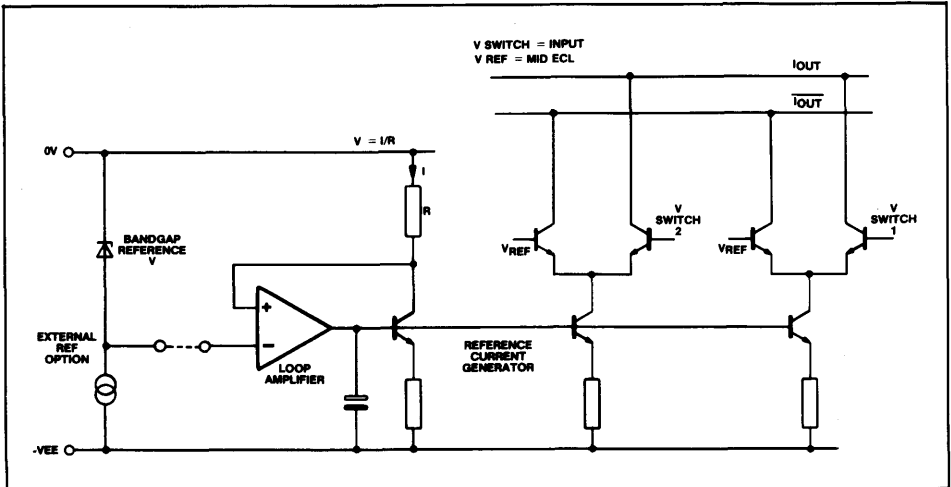


Fig.3 Basic current switch DAC technique :

**OPERATION**

The pinout of the device is shown in Fig.1. External components are current setting resistor and a decoupling capacitor.

The DAC has current outputs, with a nominal full-scale of 20mA, corresponding with a 1 volt drop across a 50Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current,  $I_{OUT}$ , is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary  $I_{OUT}$  is also provided. If single output operation only is employed it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor,  $R_{SET}$ , is typically 240Ω, giving a full-scale output current of 21mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally 1.280 volts and is of a modified bandgap type. Samples show average

temperature coefficients of 50ppm/°C over the range -55°C to +125°C. This precision voltage reference can be used as an independent part.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled to ground with a 1nF ceramic chip capacitor. The current loop technique has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

Fig.2(a) shows a suggested circuit for a conventional D to A using the on-chip voltage reference.

**Multiplying mode**

Multiplying operation of the DAC is available in two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3dB bandwidth is 250kHz, while in the latter, operational use exceeds 20MHz. A suggested circuit is shown in Fig.2(b).

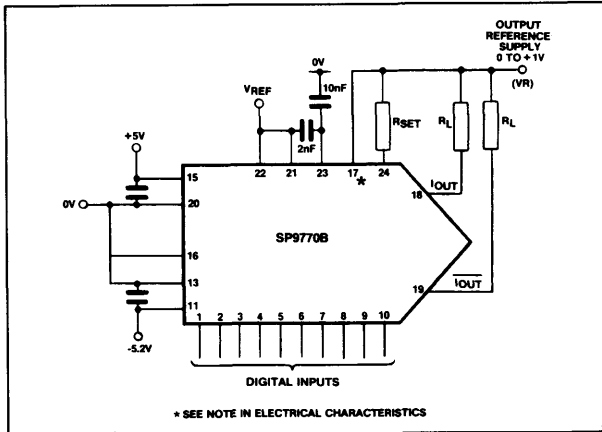


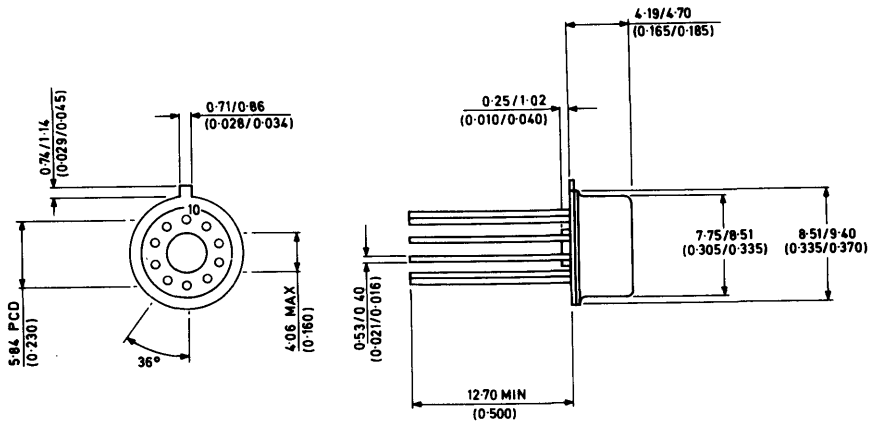
Fig.4 Voltage output referred to a positive voltage



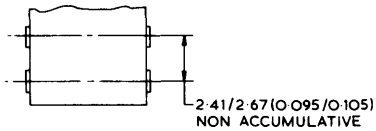
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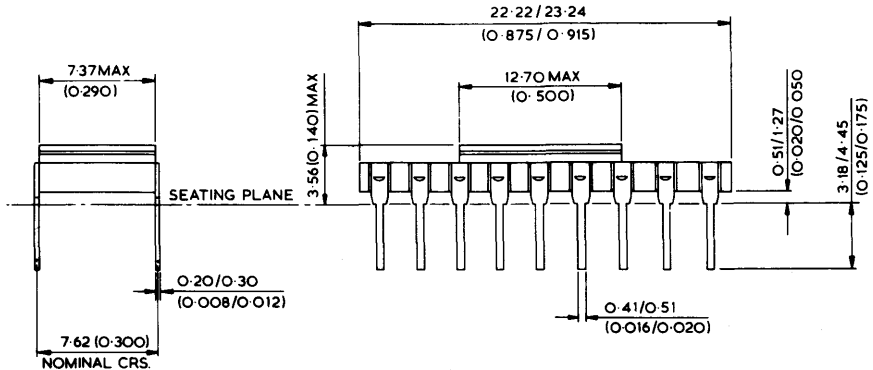




**10 LEAD TO-100 (5.84 mm PCD) WITH STANDOFF CM10/S**

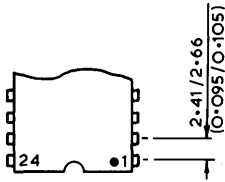


2.41/2.67 (0.095/0.105)  
NON ACCUMULATIVE



**18 LEAD DILMOM**

**DC18**



2.03/4.19  
(0.080/0.165)

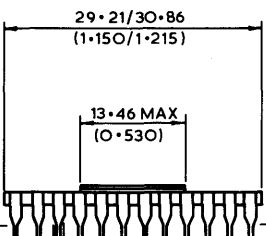
15° MAX

15.24 CRS.NOM  
(0.60)

0.51/2.03  
(0.020/0.080)

0.20/0.30  
(0.008/0.012)

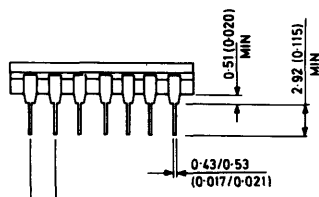
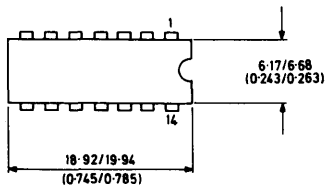
3.18/4.45  
(0.125/0.175)



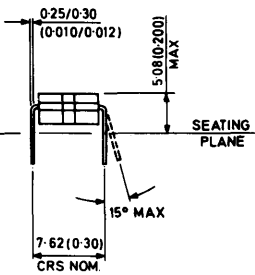
SEATING PLANE

**24 LEAD DILMON**

**DC24**

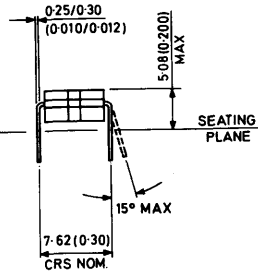
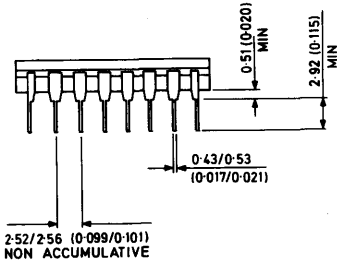
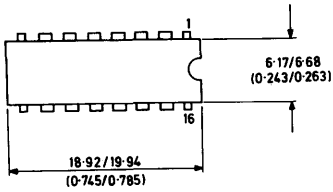


2.52/2.56 (0.099/0.101)  
NON ACCUMULATIVE



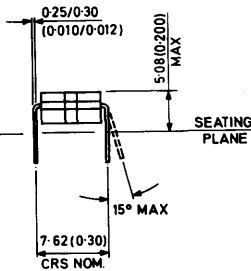
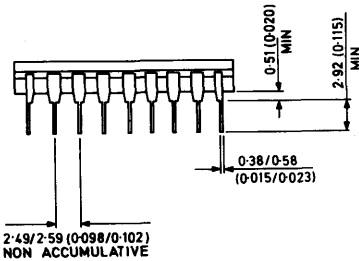
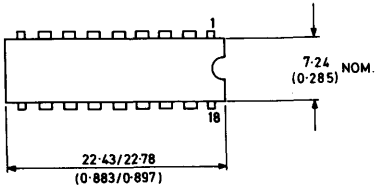
**14 LEAD CERAMIC DIL**

**DG14**



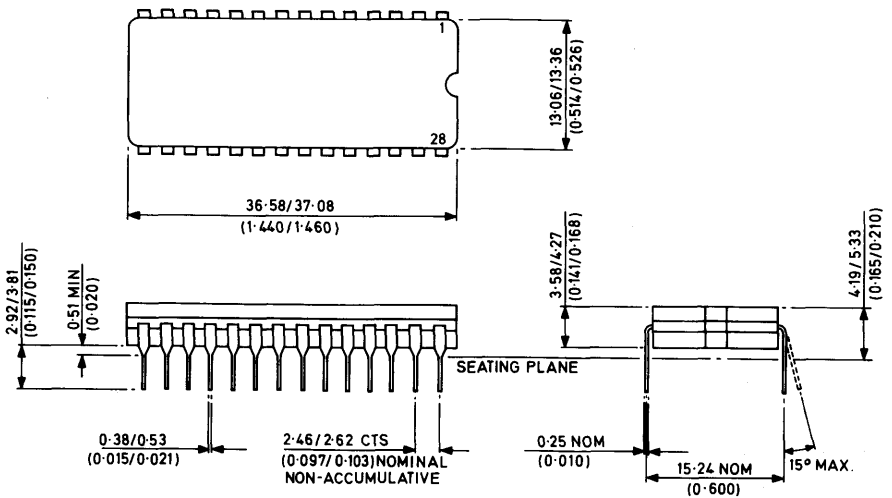
**16 LEAD CERAMIC DIL**

**DG16**



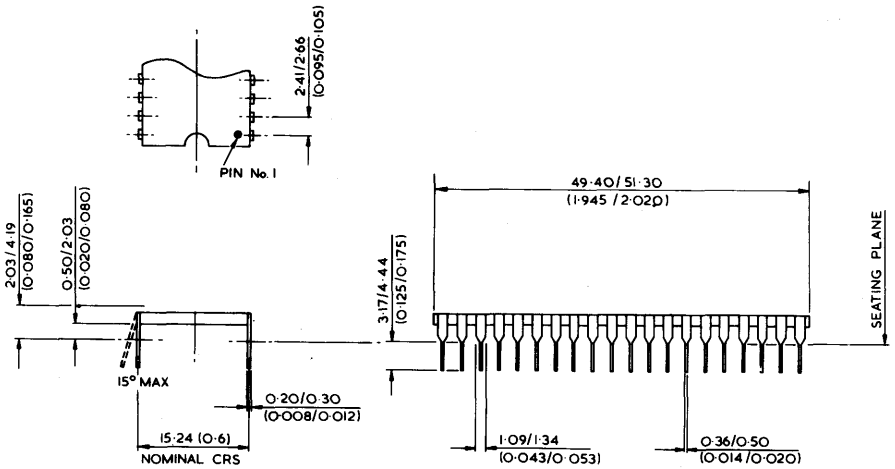
**18 LEAD CERAMIC DIL**

**DG18**



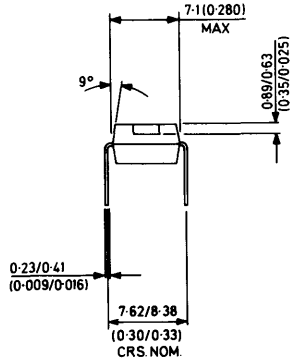
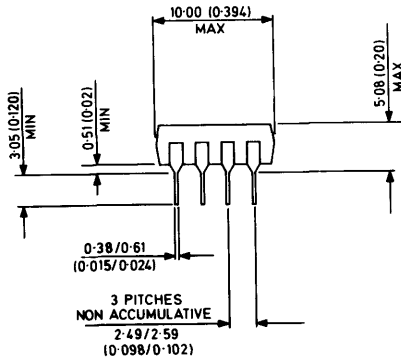
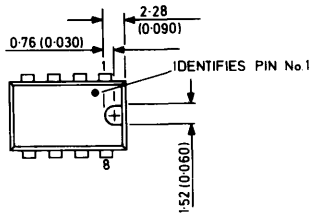
**28 LEAD CERAMIC DIL**

**DG28**



**40 LEAD CERAMIC DIL**

**DG40**



**8 LEAD PLASTIC DIP**

**DP8**



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